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**RELAXATION OSCILLATORS BASED ON  
CURRENT-CONTROLLED NEGATIVE RESISTANCE**

**A Thesis Submitted in  
Partial Fulfilment of the Requirements  
For the Degree of**

**MASTER OF TECHNOLOGY**

**by  
R. Kumar**

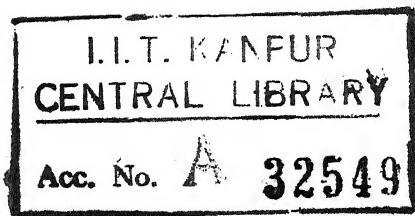
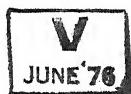
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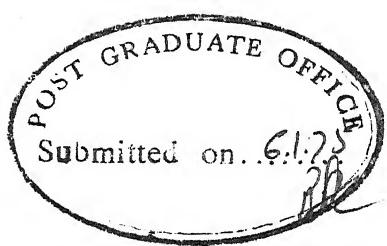
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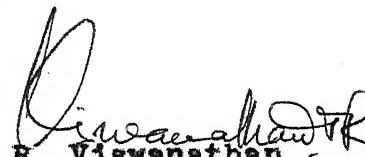
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CERTIFICATE

This is to certify that the thesis, entitled,  
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NEGATIVE RESISTANCE is a record of the work carried  
out under my supervision and that it has not been  
submitted elsewhere for a degree.

Kanpur  
December 1974

  
T.R. Viswanathan

Professor

Department of Electrical Engineering  
Indian Institute of Technology, Kanpur

POST GRADUATE OFFICE

This thesis has been approved  
for the award of the Degree of  
Master of Technology (E.I.Tech.)  
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## CHAPTER 1

### INTRODUCTION

Low frequency (1 Hz - 100 Hz) relaxation oscillators find many applications. For example, the most vital part of an electronic wrist-watch or a cardiac pace-maker is a stable low-frequency oscillator. Such oscillators are also used in the firing circuits of SCRs in power electronics applications and industrial timers.

The presented work is an attempt to investigate reliable and stable low frequency oscillators for these applications. The major requirements of such an oscillators are: small size, low power consumption, frequency stability with respect to ambient temperature and power supply voltage and simplicity of circuit for higher reliability and low cost.

Oscillator circuits based on two terminal negative resistance devices are well known for their simplicity. Thus, the use of a negative resistance device is considered in detail for application as a relaxation oscillator, to meet these requirements.

A current controlled negative resistance device is preferred over a voltage controlled negative resistance device since the former requires a capacitor for oscillations whereas the latter needs an inductor.

Small size can readily be achieved by fabricating the circuit in integrated circuit form (except for the timing elements).

The present day technique of obtaining stable low frequency oscillations is to start with a stable crystal oscillator. This requires a rather complex count-down circuitry [1] [2]. The aim of the project is to design relaxation oscillators which oscillate in the range  $1\text{Hz}$ . This obviates the need for count-down circuits.

The stability in frequency that can be achieved by this direct method is investigated with the view to determine the limits that can be achieved. In other words, the causes of instability are examined in detail and compensation schemes are tried to reduce sensitivity of frequency with respect to variation in circuit parameters arising from changes in ambient temperature and power supply voltage.

## CHAPTER 2

### RELAXATION OSCILLATOR

#### 2.1 Piece-wise Linear Current-Controlled Negative Resistance

Let us assume that we have a piece-wise linear current controlled negative resistance device (CCNR) whose terminal characteristics are shown in Figure (2.1). It is well known that relaxation oscillations are readily obtained by using the NR device in the circuit configuration shown in Figure (2.2). The period of oscillations of the circuit is derived in terms of the circuit and device parameters.

#### 2.2 Bias Condition

The supply voltage  $E$  and resistance  $R_L$  are chosen in such a way that the load line intersects the characteristics at a single point Q (Figure 2.1) on the negative resistance region of the characteristics. Since, at the point Q, the circuit is unstable, a small perturbation will cause the circuit to oscillate and the trajectory of the operating point will be as shown in Figure (2.1) [A B C D A]. In other words, the point of operation will move along this trajectory. The time taken for one period will now be evaluated in terms of the time taken for the operating point to traverse the segments AB, BC, CD and DA.

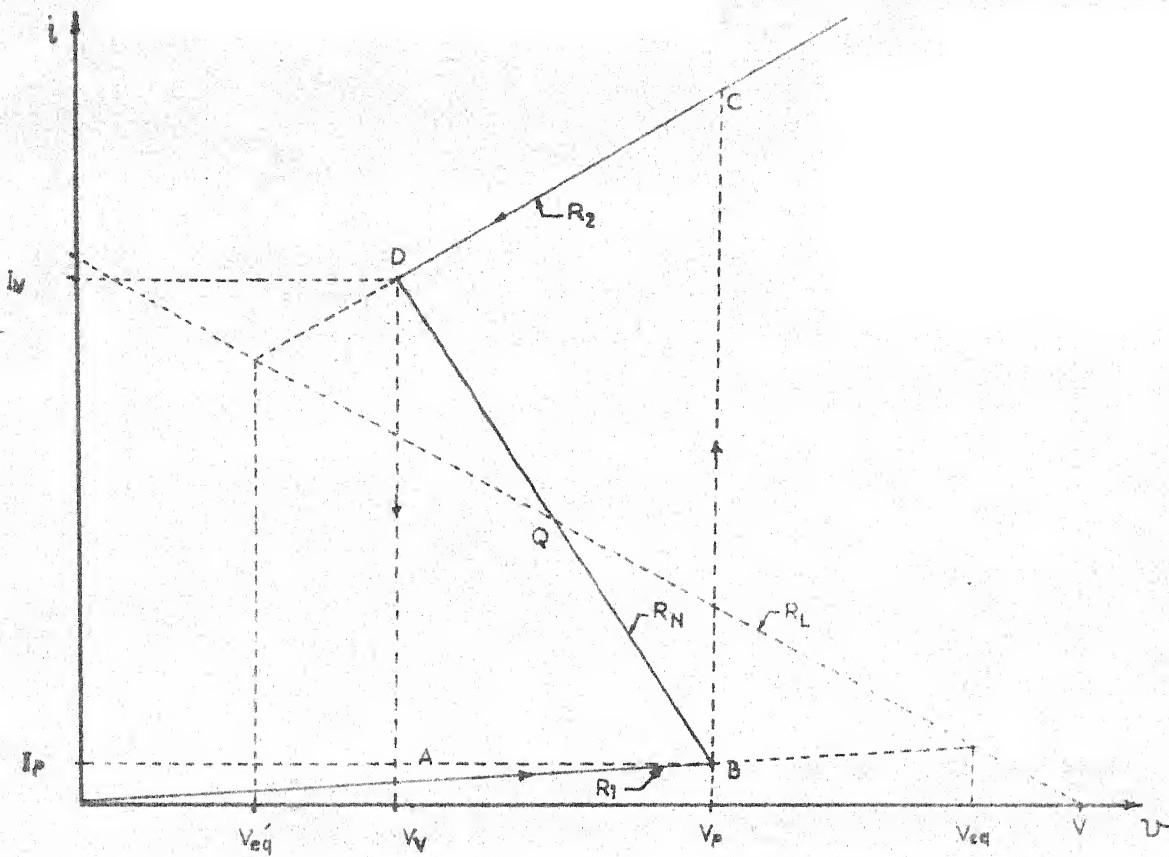


FIG. (21)

PIECE-WISE LINEAR CCNR CHARACTERISTICS

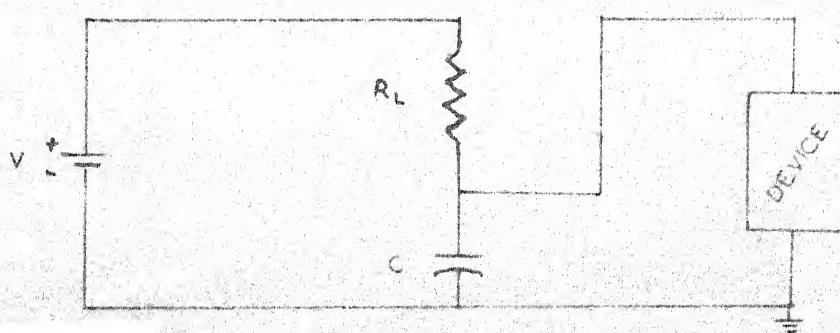


FIG.(22)

SIMPLE OSCILLATOR CIRCUIT USING CCNR DEVICE

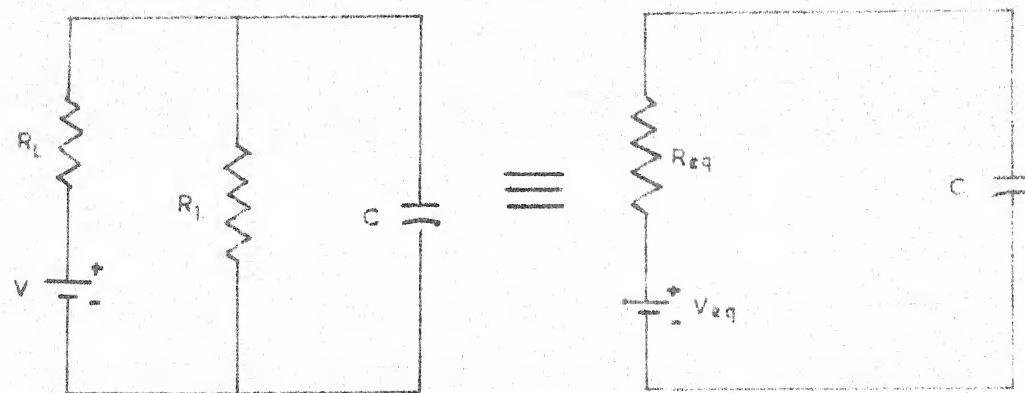


FIG. (2.3)

EQUIVALENT CIRCUIT FOR THE SEGMENT AB

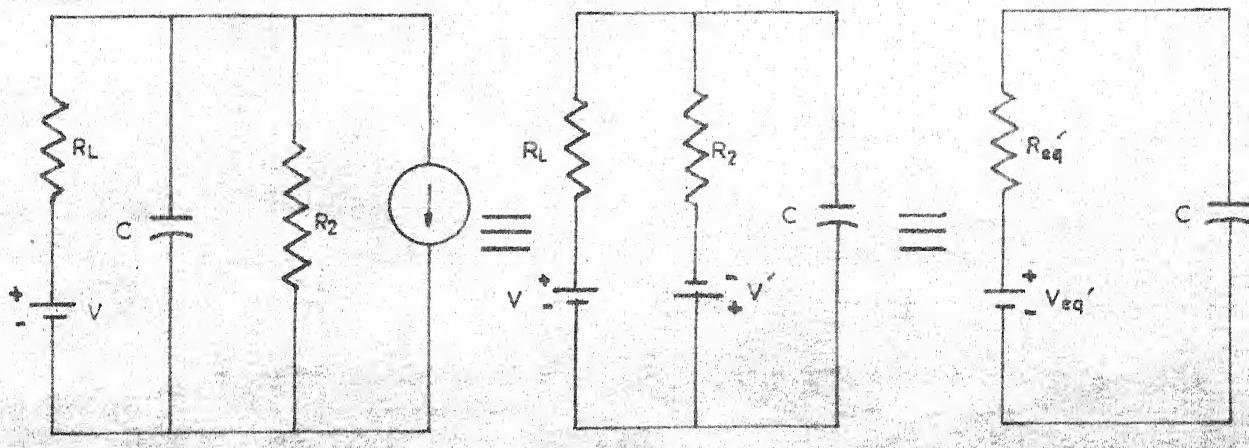


FIG. (2.4)

EQUIVALENT CIRCUIT FOR THE SEGMENT CD

### 2.3 Time Period

It can be seen that the circuit switches rather abruptly from B to C and from D to A. These switching times are relatively small and are neglected in the analysis.

When the operating point is traversing the segment AH, the device can be replaced by a simple equivalent circuit shown in Figure (2.3) and the time  $T_1$ , taken by the operating point to move from A to E is obtained as follows:

$$\text{Let } V_{eq} = \frac{V \times R_1}{R_1 + R_L} \quad \text{and} \quad R_{eq} = \frac{R_1 \times R_L}{R_1 + R_2} \quad (2.1)$$

For a circuit with a single time constant,

$$v(t) = V_{final} + (V_{initial} - V_{final})e^{-t/\tau} \quad (2.2)$$

where  $\tau$  is time constant of the circuit.

With reference to Figure (2.1) set

$$V = V_v \text{ for } t = 0 \quad \text{and} \quad V = V_{eq} \text{ for } t = \infty$$

Thus

$$v(t) = V_{eq} + (V_v - V_{eq})e^{-t/CR_{eq}}$$

If the time taken for the operating point to traverse the segment AB is  $T_1$ , we can write

$$V_p = V_{eq} + (V_v - V_{eq})e^{-T_1/(CR_{eq})}$$

or

$$T_1 = CR_{eq} \times \ln \left( \frac{V_{eq} - V_p}{V_{eq} - V_v} \right) \quad (2.3)$$

Similarly for the segment  $C_D$ , the device can be replaced by a resistance  $R_2$  in parallel with a current source of magnitude  $I_o$ . The equivalent circuit of the device is shown in Figure (2.4).

Where

$$V' = I_o \times R_2, V'_{eq} = \frac{VR_2 - V'R_L}{R_2 + R_L}$$

and

$$R'_{eq} = \frac{R_L \parallel R_2}{R_L + R_2} \quad (2.4)$$

Again using Equation (2.2) and setting

$$v = V_p \text{ at } t = 0 \quad \text{and} \quad v = V'_{eq} \text{ at } t = \infty$$

we get

$$v(t) = V'_{eq} + (V_p - V'_{eq})e^{-t/CR'_{eq}}$$

If  $T_2$  is the time taken by the operating point to traverse the segment  $CD$ , we can write

$$v_v = V'_{eq} + (V_p - V'_{eq})e^{-T_2/CR'_{eq}}$$

or

$$T_2 = CR'_{eq} \ln \left( \frac{V_p - V'_{eq}}{V_v - V'_{eq}} \right) \quad (2.5)$$

The period of oscillations  $T = T_1 + T_2$  will be given by

$$T = CR'_{eq} \ln \left( \frac{V'_{eq} - V_v}{V'_{eq} - V_p} \right) + CR'_{eq} \ln \left( \frac{V_p - V'_{eq}}{V_v - V'_{eq}} \right) \quad (2.6)$$

If a stable relaxation oscillator is to be obtained it will be necessary for the period to be insensitive to variation in the ambient temperature and variation in the supply voltage.

## 2.4 Effect of Variation of Supply Voltage

From Equation (2.3)

$$T_1 = CR_{eq} \ln \left( \frac{V_{eq} - V_v}{V_{eq} - V_p} \right)$$

If  $V_v$  and  $V_p$  are of the form

$$V_v = K_1 V, V_p = K_2 V \text{ and } V_{eq} = \frac{R_1 V}{R_1 + R_L} = K_3 V,$$

$$T_1 = CR_{eq} \ln \left( \frac{K_3 V - K_1 V}{K_3 V - K_2 V} \right) = CR_{eq} \ln \left( \frac{K_3 - K_1}{K_3 - K_2} \right)$$

(2.6)

The value of  $V_{eq}$  in terms of  $R_2, R_N, R_L, V_p, V_v$  and  $V$  is determined below.

From Figure (2.1)  $V_{eq}$  is the point of intersection of lines representing  $R_1$  and the loadline  $R_L$ . Equation for the load line  $R_L$  is

$$v = V - i \times R_L \quad (2.8)$$

Now

$$I_v = \frac{V_p - V_v}{R_N} + \frac{V_p}{R_1}$$

Therefore Equation for the segment CD is given by

$$u = v_v + [i - \left( \frac{V_p - V_v}{R_N} + \frac{V_p}{R_1} \right)] R_2 \quad (2.9)$$

Solving Equation (2.8) and (2.9) simultaneously and eliminating  $i$  we get the value of  $V_{eq}$

$$V_{eq}' = V_V + \left[ \frac{V - V_{eq}'}{R_L} - \frac{V_P - V_V}{R_N} + \frac{V_P}{R_1} \right] R_2$$

or

$$V_{eq}' = \frac{R_1}{R_2 + R_L} [V_V - \frac{R_N + R_2}{R_N} - V_P \frac{R_1 + R_N}{R_1 + R_N}] R_2 + \frac{V_R P}{R_N}$$

Since,  $R_2$ ,  $R_N$  and  $R_L$  are fixed and  $V_V$  and  $V_P$  are proportional to supply voltage  $V$ ,  $V_{eq}'$  can be expressed as

$$V_{eq}' = K_4 V$$

substituting for  $V_P$ ,  $V_V$  and  $V_{eq}'$  in Equation (2.5) we get

$$T_2 = CR_{eq}' \ln \frac{K_2 - K_4}{K_1 - K_4} \quad (2.10)$$

Total time period from Equation (2.7) and (2.10)

$$T = T_1 + T_2$$

$$= CReq \ln \frac{K_3 - K_1}{K_3 - K_2} + CReq' \ln \frac{K_2 - K_4}{K_1 - K_4} \quad (2.11)$$

If  $Req$ ,  $Req'$  and  $C$  are constant it can be seen that supply voltage variation will not effect the period of oscillation.

### 2.5 Effect of Variation of Temperature

It is clear from Equations (2.6) (2.1), (2.4) that  $C$ ,  $R_1$  and  $R_2$  should have a very low temperature coefficients to obtain a stable oscillator.

The design of a circuit with a piece-wise linear i-v characteristics where  $V_p$ ,  $V_V$ ,  $R_1$ ,  $R_2$  and  $R_N$  are controlled externally will now be discussed.

## 2.6 Basic Negative Impedance Converter

A simple circuit configuration [3] is shown in Figure (2.5). The input current  $I$  forms the emitter current of the transistor  $T_1$ . A dependent current source ( $I_{C2} = nI_{C1}$ ) whose magnitude is linearly related to the collector current of the transistor  $T_1$  is obtained by the diode-transistor combination  $D_2, T_2$ . The arrangement where the diode is a diode connected <sup>transistor</sup> has temperature compensating features and is widely used in the integrated circuits. This combination is widely known as the current mirror. The additional diode connected transistor  $D_1$  compensates for the voltage drop across the emitter-base junction of the transistor  $T_1$ , provided the transistors are identical and the current through diode  $D_1$  is equal to the input current  $I$ . Under these conditions, the voltage across the input and output parts will be equal, resulting in current inversion type Negative Impedance Converter (NIC).

## 2.7 i-V Characteristics

The i-v characteristics of NIC, looking into node A can be studied by assuming a current  $I$ , flowing into the node A. Neglecting (for the time being), the voltage drops across the resistor  $R_N$  and the diode  $D_1$  due to the leakage currents of the reverse-biased collector-base junctions of  $T_1$  and  $T_2$ , the potential at the base of the transistor  $T_1$  is  $V_p$ . As long as the voltage at

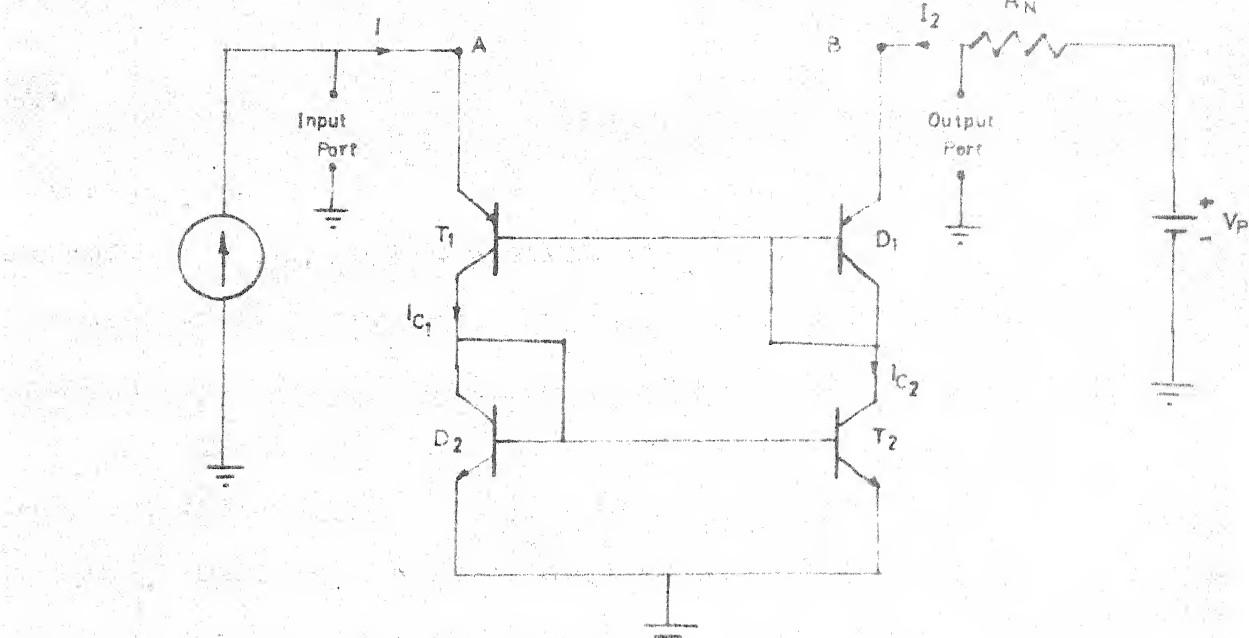


FIG. (25)  
SIMPLE NIC CIRCUIT

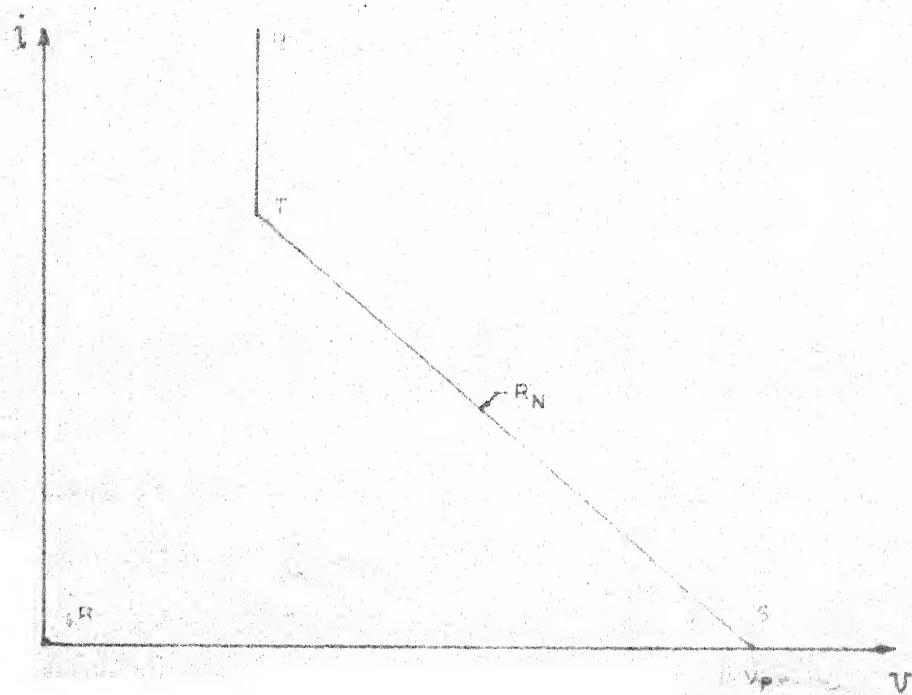


FIG. (26)  
TERMINAL CHARACTERISTICS OF THE NIC

the node A is less than  $V_p$ , the emitter-base junction of the transistor  $T_1$  is reverse biased and the transistor is cut off. Thus, except for leakage currents, there is no current flowing in the diode  $D_2$  and hence no current flows in the transistor  $T_2$  as well. Neglecting the reverse saturation current of the emitter-base junction of  $T_1$ , the i-v characteristics upto a voltage  $V_p$  is represented by the segment RS (Figure 2.6B).

When the voltage at the node A goes above  $V_p$ , the emitter-base junction of the transistor  $T_1$  is forward biased and the collector current of  $T_1$  flows through diode  $D_2$  which turns on the transistor  $T_2$ .

If the diode-connected transistor  $D_2$  and the transistor  $T_2$  are matched then

$$\frac{I_{c2}}{I_{c1}} = \frac{\beta}{\beta+2} \quad (2.12)$$

where  $\beta$  is common-emitter current gain of the npn transistors.

It is clear that as  $I$  is made to increase,  $I_2$  increases proportionately. Since the voltage at node B is  $(V_p - I_2 R_N)$ , it continues to fall as  $I_2(nI_1)$  increases; till the transistors saturate. If equal currents flow through  $D_1$  and  $T_1$  and if  $D_1$  and emitter-base junction of  $T_1$  are matched, the voltage at the node A will be equal to voltage at node B.

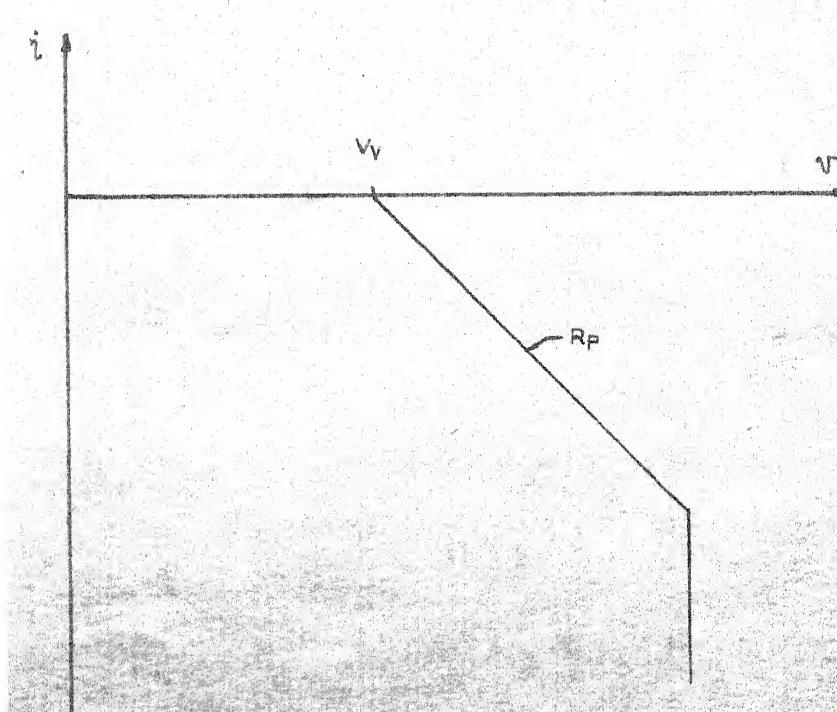
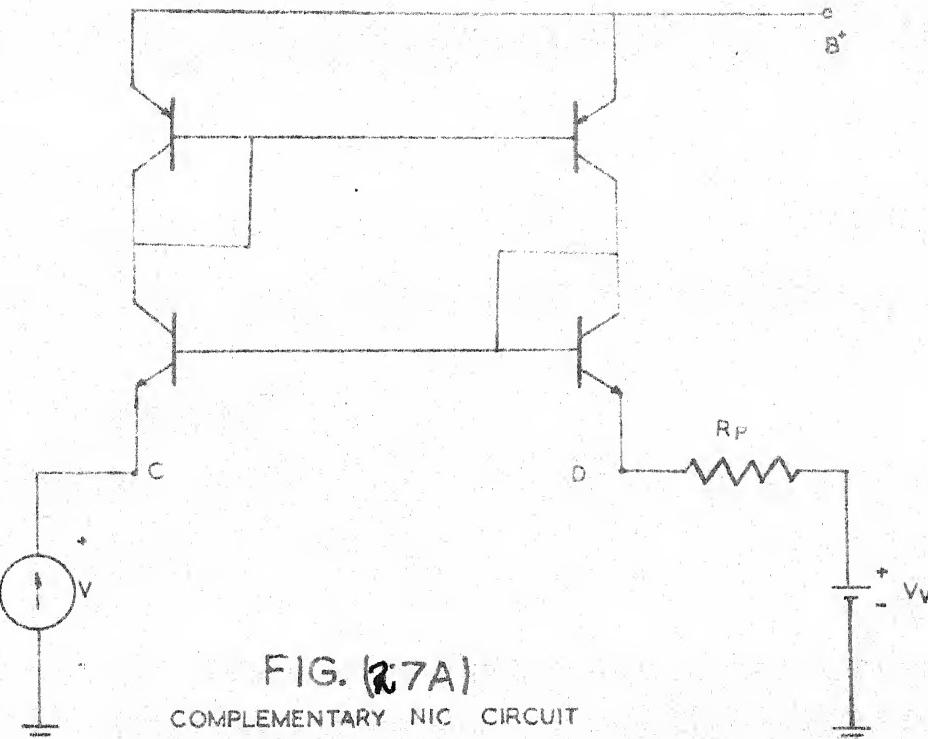


FIG.(2.7B)  
TERMINAL CHARACTERISTICS OF COMPLEMENTARY NIC

Hence the i-v characteristics of the device after the transistors conduct are represented by segment STU (Figure 2.6B). If the base current of the transistors  $T_1$  and  $T_2$  are neglected,  $I_2$  will be equal to 1 and the resistance w/  $R_N$  will appear as a negative resistance of magnitude  $R_N$  at the input port.

A complementary circuit arrangement is shown in Figure (2.7A). It can be easily seen that, looking at the node C, the circuit will have the terminal characteristics given in Figure (2.7B).

### 2.8 Two Terminal Current-Controlled Negative Resistance Device

The circuits of Figures (2.6A) and (2.7A) can be combined as shown in Figure (2.8A) to obtain a current-controlled negative resistance (CCNR) device. It is assumed that  $V_p > V_v$  and  $R_N > R_p$ .

### 2.9 i-v Characteristics

As I is increased from zero, circuit (2) remains cut off ( $V_p$  being greater than  $V_v$ ) till the voltage at node B falls below  $V_v$ . As the input current is increased further the potential at nodes A and B will go below  $V_v$  and the circuit (2) becomes active and the net resistance (R) from node B is given by

$$R = \frac{-R_p \times R_N}{R_N - R_p} \quad (2.13)$$

If  $R_N > R_p$ , R is a negative resistance which appears as a positive resistance at node A (Figure 2.8A).

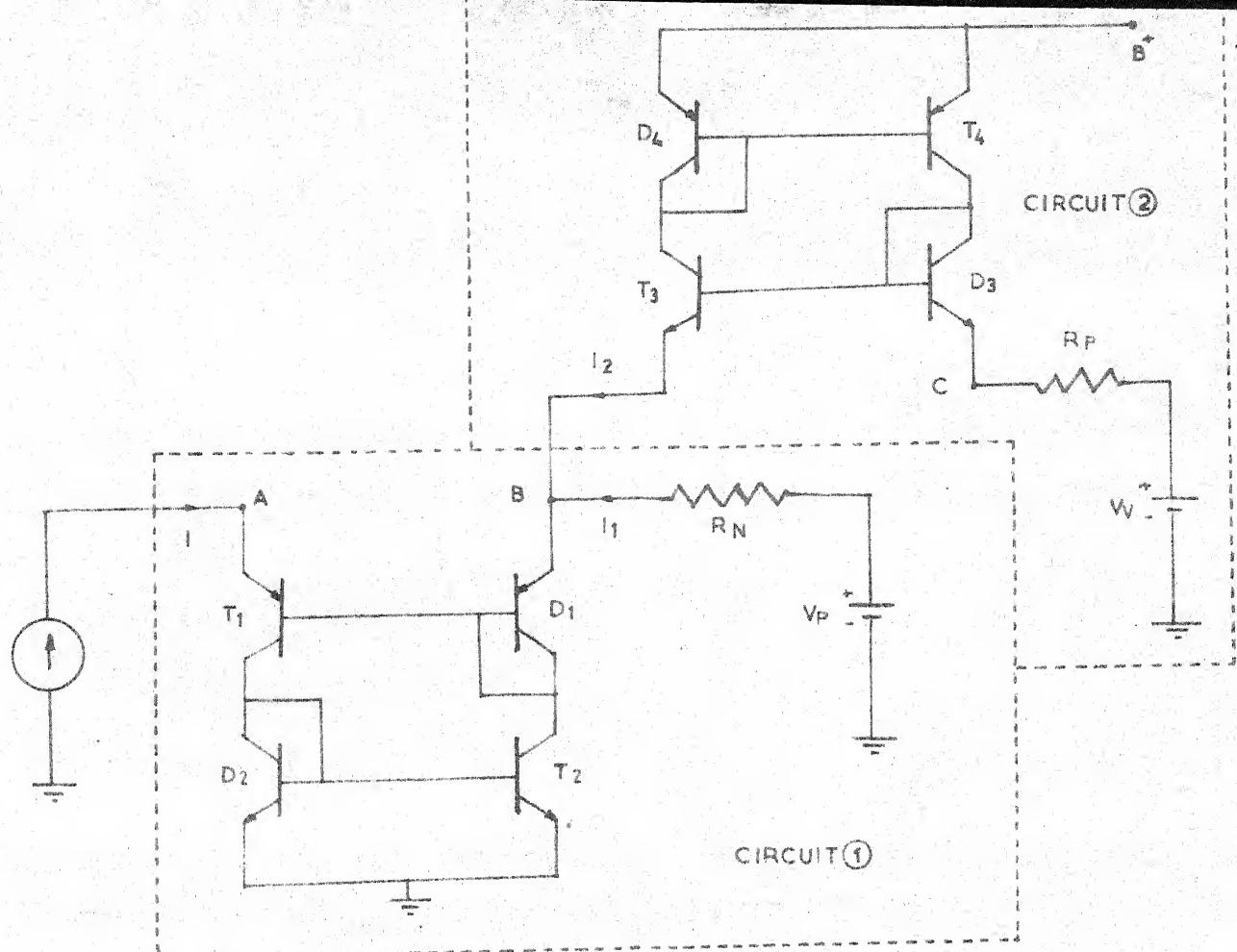


FIG. (2.8A)  
COMBINED CCNR CIRCUIT

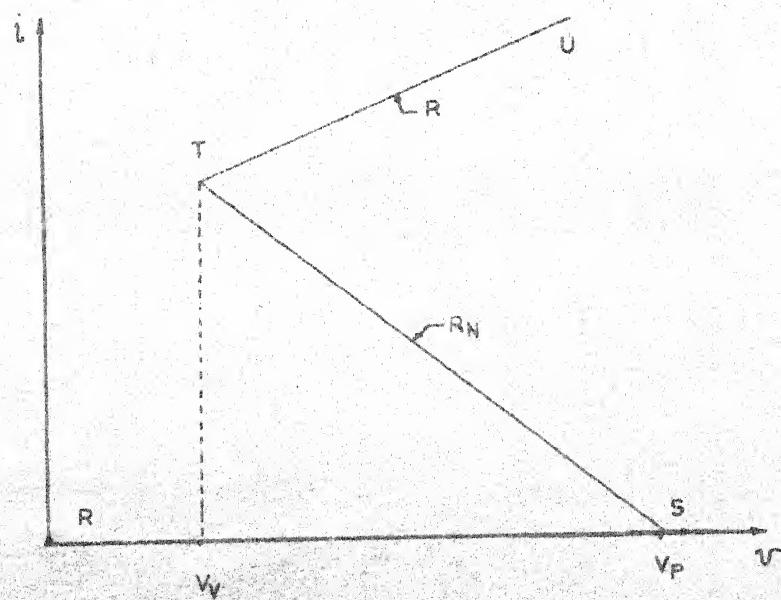


FIG. (2.8B)  
TERMINAL CHARACTERISTICS OF THE COMBINED CCNR CIRCUIT

The circuit, thus, will have the characteristics shown in Figure (2.8B).

## CHAPTER 3

### CIRCUIT REALIZATION

#### 3.1 Choice of Devices

The CCNR device shown in Figure (3.1) was constructed with monolithic transistor arrays CA 3083 for npn transistors and CA 3084 for pnp transistors. These arrays provide matched devices on the same chip which ensure close thermal coupling and hence tracking of device parameters with temperature. The specifications of these are given in Appendix A. Precision metal film resistors are used to control the characteristics as well as defining  $V_p$  and  $V_v$ .

#### 3.2 Overshoot Around $V_p$

In our earlier qualitative description of the circuit behaviour given in Section 1.31, we had neglected the leakage currents as well as the base currents of the transistors. Now we shall examine the influence of these currents.

With reference to Figure (3.2A) the reverse saturation current  $I_{CO1}$  and  $I_{CO2}$  of the collector-base junctions of the transistors  $T_1$  and  $T_2$  flow as shown explicitly in the figure. The sum of these currents flow in the diode  $D_2$ . This results in an equal emitter current in  $T_2$ . The corresponding collector current as well as  $(I_{CO1} + I_{CO2})$

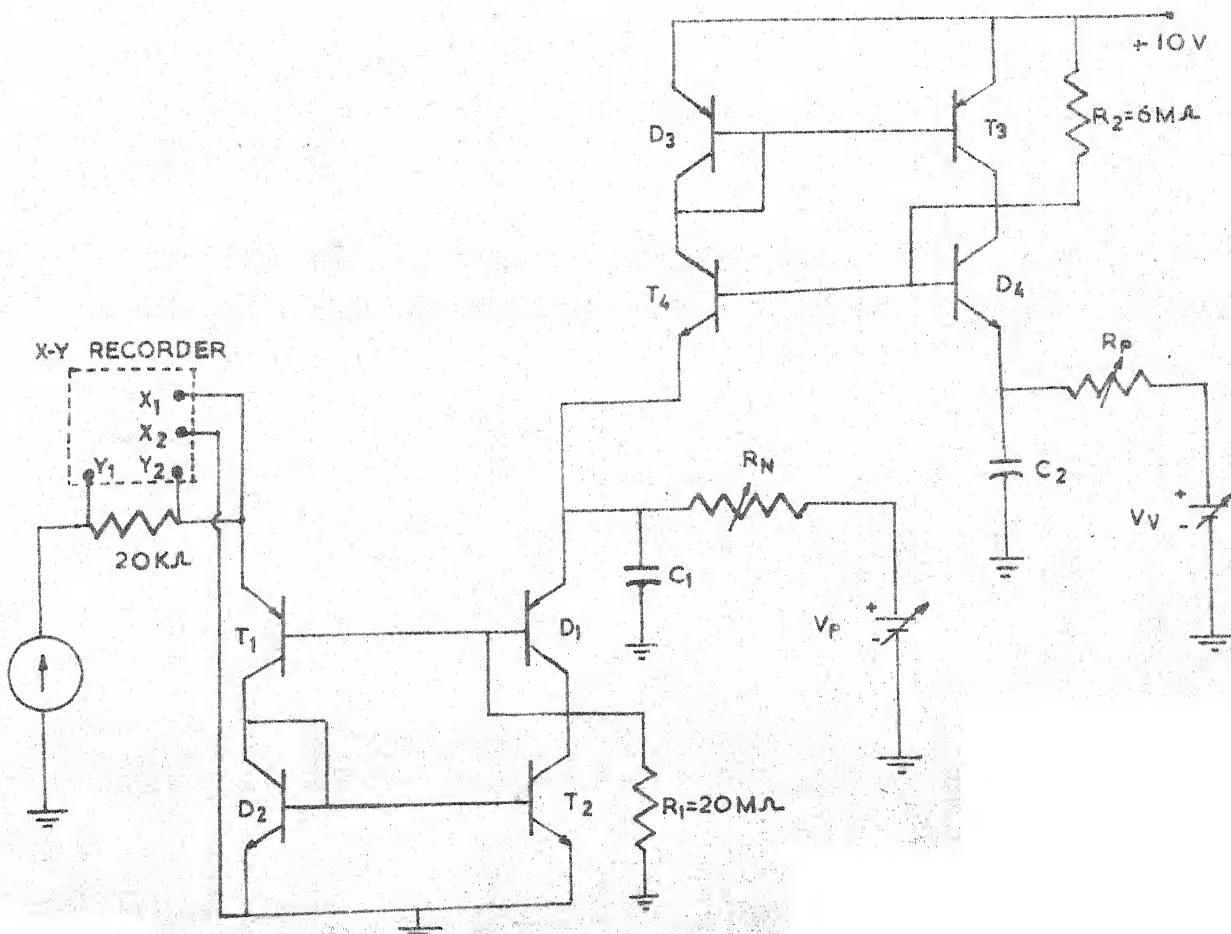


FIG. (3.1)

CIRCUIT REALIZATION USING TRANSISTOR ARRAYS

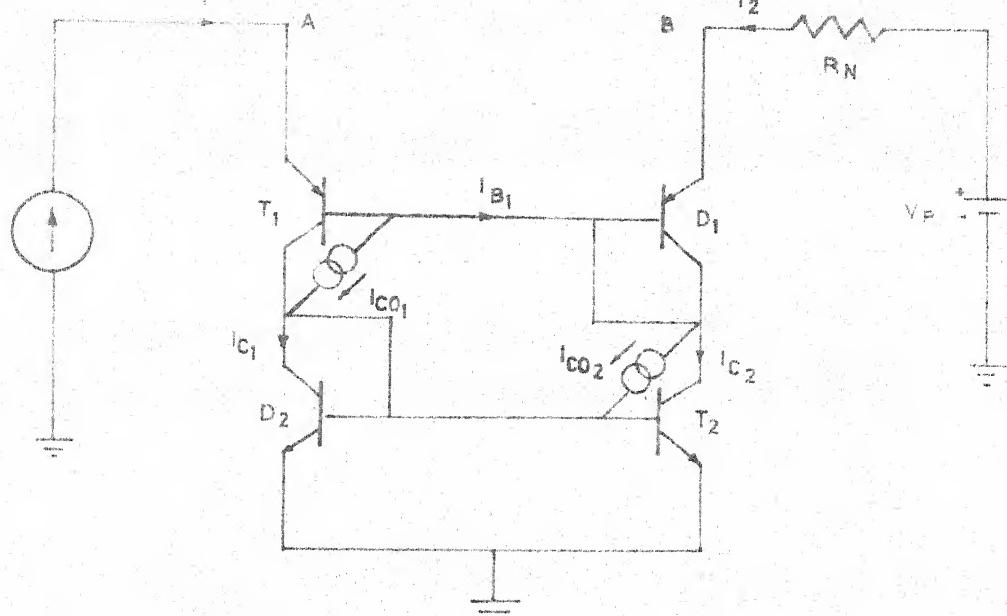


FIG. (3.2A)

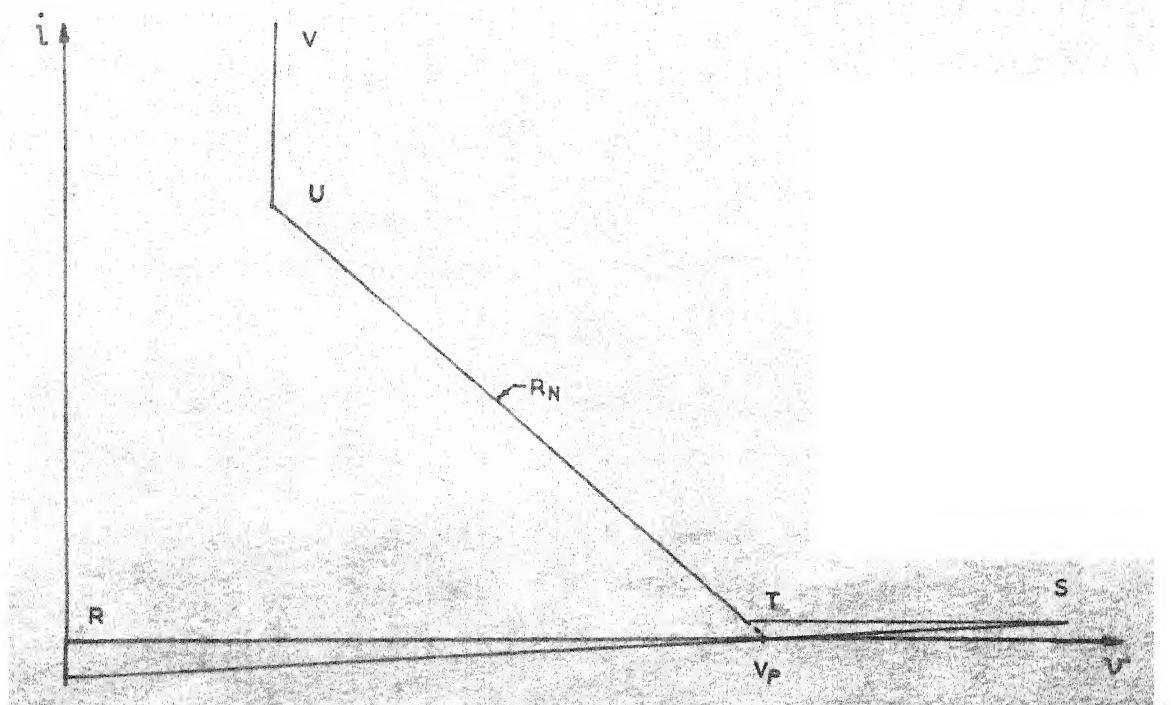
INFLUENCE OF BASE CURRENTS AND  $I_{CO_1}$  AND  $I_{CO_2}$ 

FIG. (3.2B)

PRACTICAL CHARACTERISTICS  
SHOWING OVERSHOOT AROUND  $V_P$

flow through  $D_1$  forward-biasing it slightly. When the voltage at the node A reaches a value when the transistor  $T_1$  just starts conducting, its  $\alpha$  is low and hence under these conditions the base current of  $T_1$  tends to be large proportion and very little collector current would flow. Thus if  $I_{B1}$  is greater than  $I_{C2}$ , the diode  $D_1$  will be reverse biased making the input voltage increase beyond  $V_p$ . As the input current I increases, the  $\alpha$  of  $T_1$  improves, so that eventually  $I_{B1}$  becomes equal to  $I_{C2}$  (Figure 2.2A). Beyond this point the diode  $D_1$  will be forward biased and the circuit will operate as explained in Section 1.21. In other words, the practical characteristics will be as shown in Figure (3.2B).

A large resistance  $R_1$  (chosen experimentally) is connected as shown in Figure (3.1) which will slightly forward bias the diode  $D_1$  so that for low values of I, the diode  $D_1$  never gets a chance to get reverse biased. This removes the over-shoot in the characteristics beyond  $V_p$ . Similarly the resistor  $R_2$  removes the overshoot around the valley point.

### 3.3 Stabilization and Experimental Arrangement

It is well known [5] that small stray capacitances introduced between the node A and ground (due to test equipment connected at the node A) will make the circuit unstable. A simple way of stabilizing the circuit for plotting terminal i-v characteristics is to connect capacitors  $C_1$  and  $C_2$  as shown in Figure (3.1). The plots are obtained using the arrangement shown in Figure

(3.2C) and applying slowly varying currents so as to meet the quasi-static condition which makes the capacitor currents due to  $C_1$  and  $C_2$  negligibly small.

#### 3.4 Effect of Variation of $V_p$ and $V_v$

The peak voltage can be controlled by the variable power supply  $V_p$ , shown in Figure 3.1. Experimental results obtained by varying  $V_p$  are shown in Figure (3.3).

Similarly, valley voltage is controlled by varying variable power supply  $V_v$  and Figure (3.4) shows the experimental results.

#### 3.5 Effect of Variation of $R_N$

The slope of the negative resistance region can be varied by changing the value of  $R_N$  (Figure 3.5). The value of negative resistance as measured from the i-v characteristics is in agreement with that predicted by Equation 1.12.

#### 3.6 Effect of Variation of $R_p$

The slope of the positive resistance region of i-v characteristics can be controlled by varying  $R_p$ . Experimental evidence to this effect is shown in Figure 3.6.

It is observed that the characteristics are non-linear in this region. It is due to the reason that transistor T3 (Figure 3.1) is a lateral pnp device with low  $\beta$ , (of the order of 10), therefore the gain of the current mirror is highly  $\beta$  dependent. Since  $\beta$  of the transistor varies with current level as well as the collector-base reverse bias voltage, the current gain  $\frac{I_1}{I_2}$  is not constant and hence the i-v characteristics are non-linear in this region. For smaller values of  $R_p$ , the

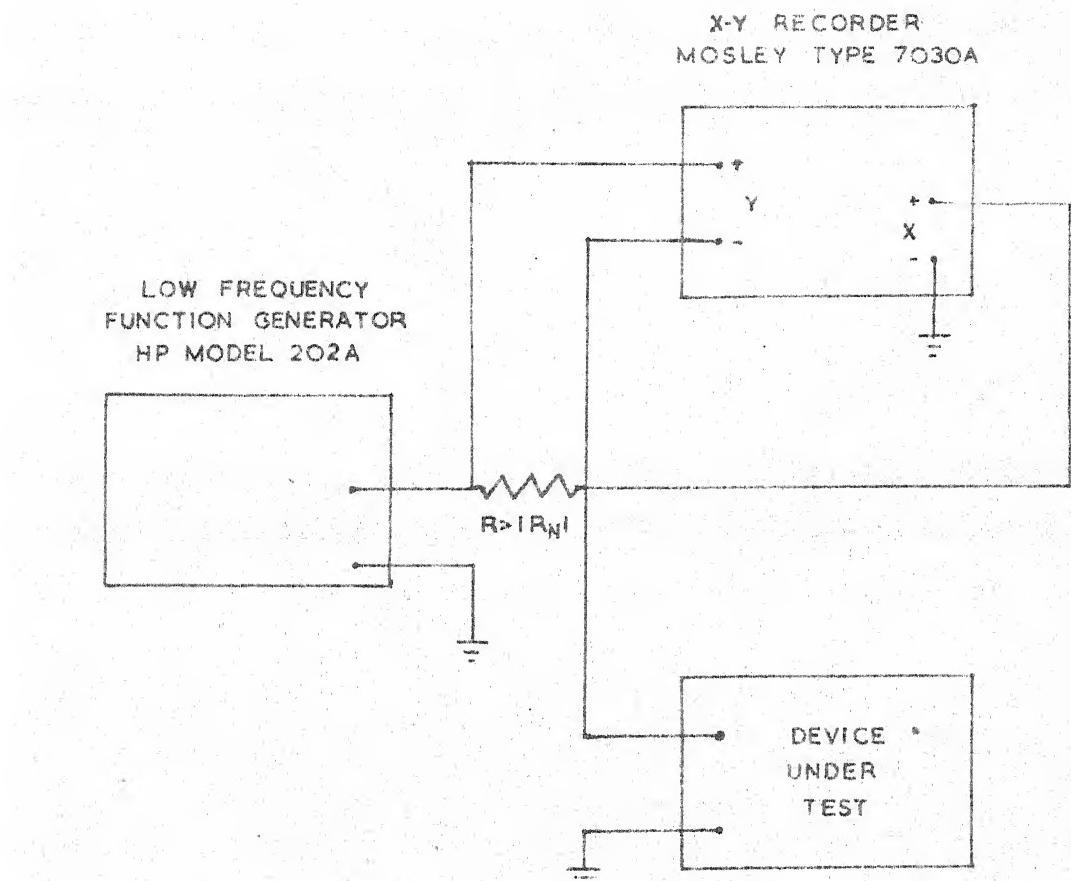
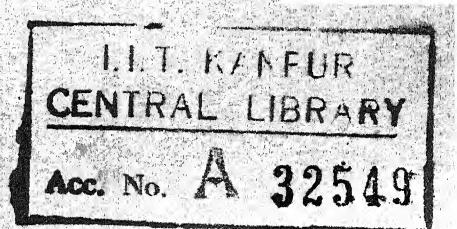
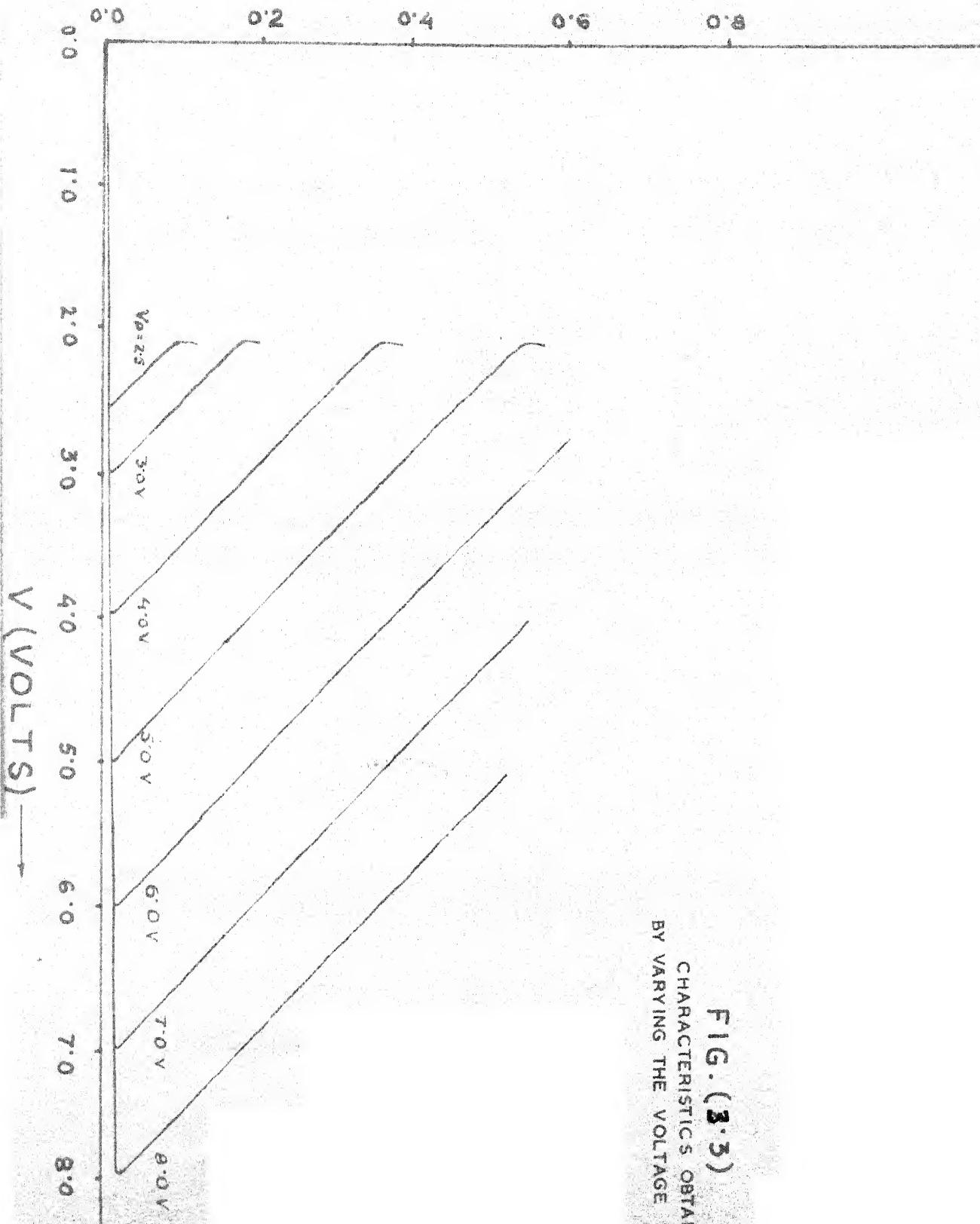


FIG. (3.2C)

EXPERIMENTAL ARRANGEMENT FOR CIRCUIT REALIZATION



I (mA) —→



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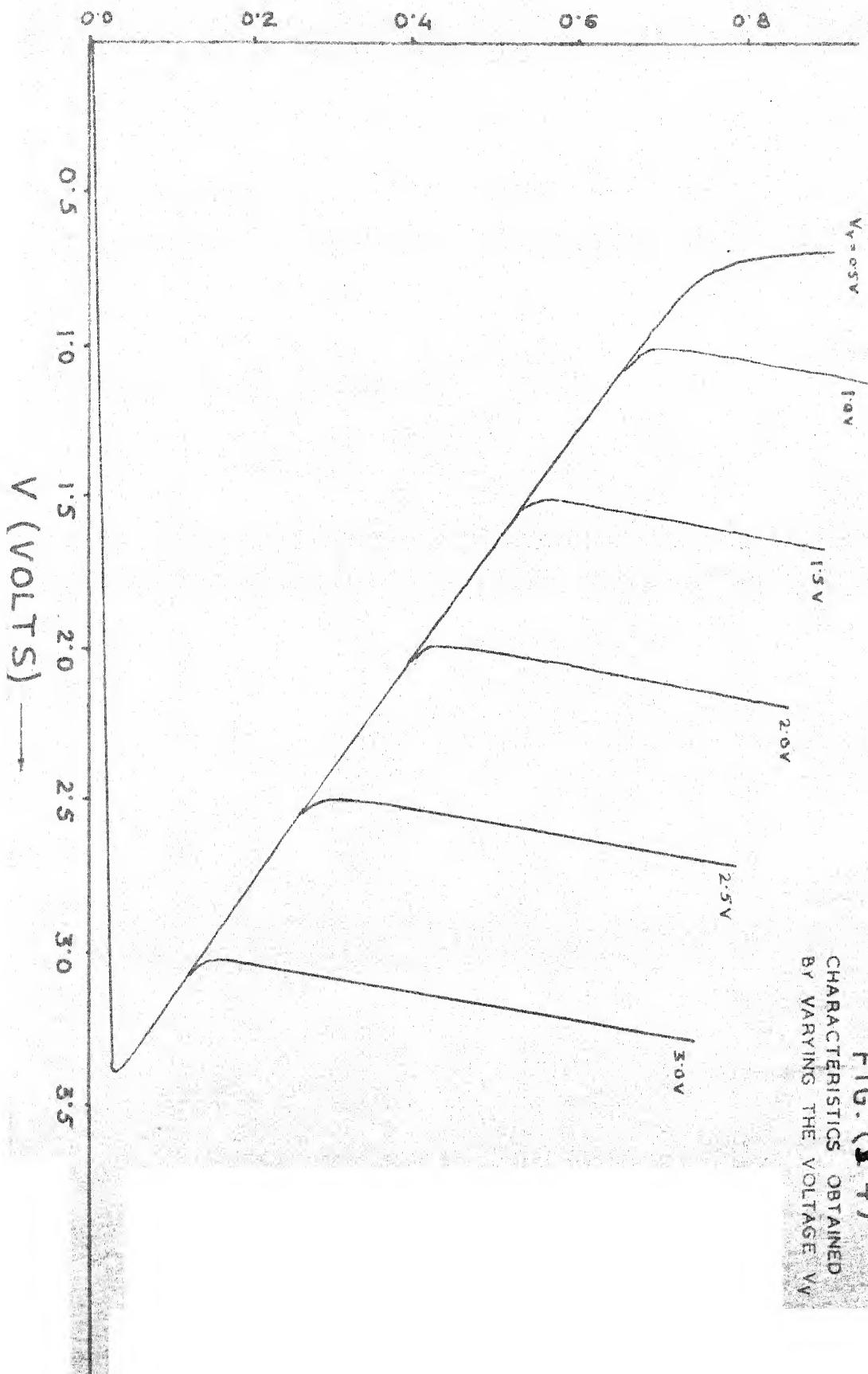
 $I$  (mA) —

FIG. (3.4)  
CHARACTERISTICS OBTAINED  
BY VARYING THE VOLTAGE  $V_V$

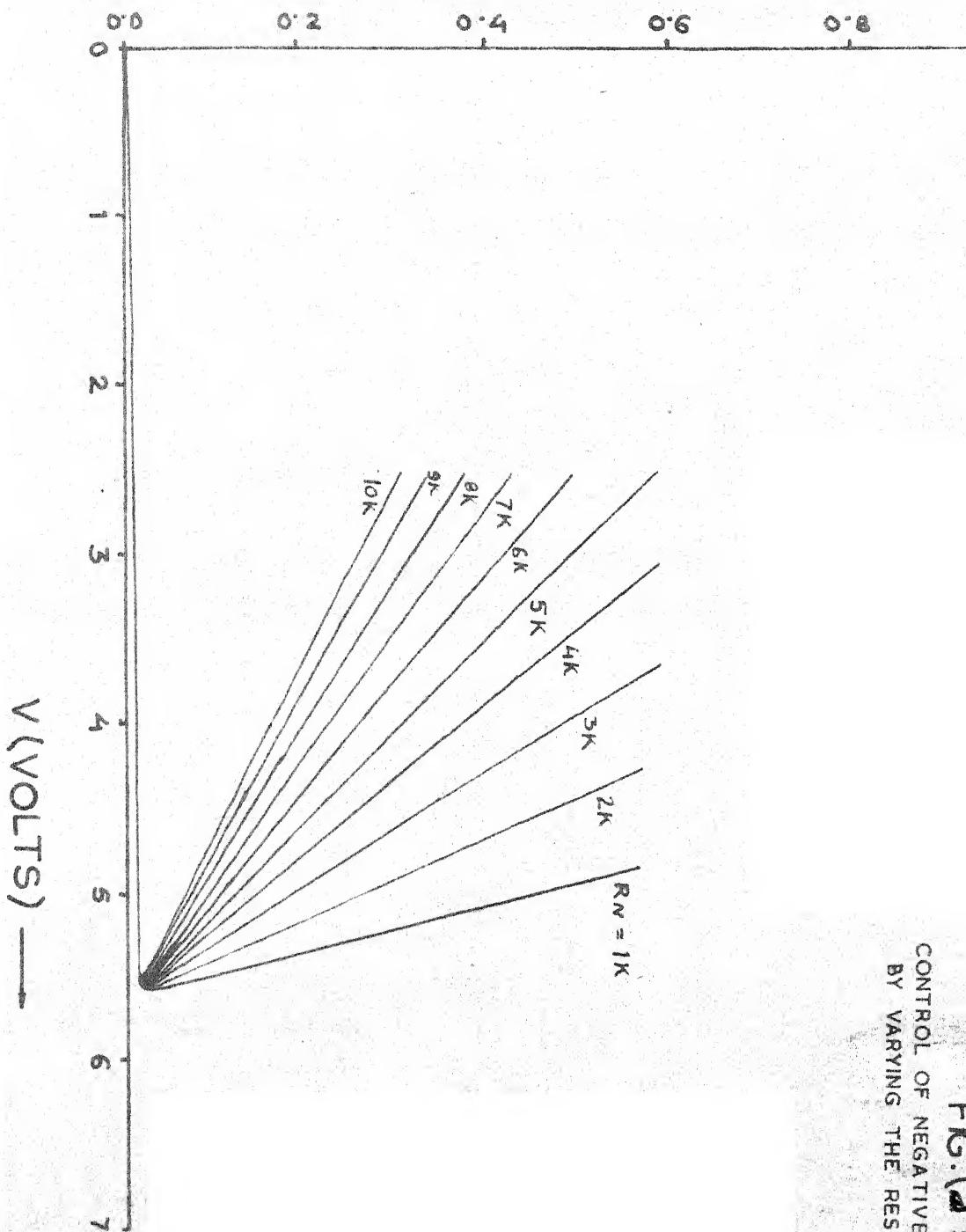
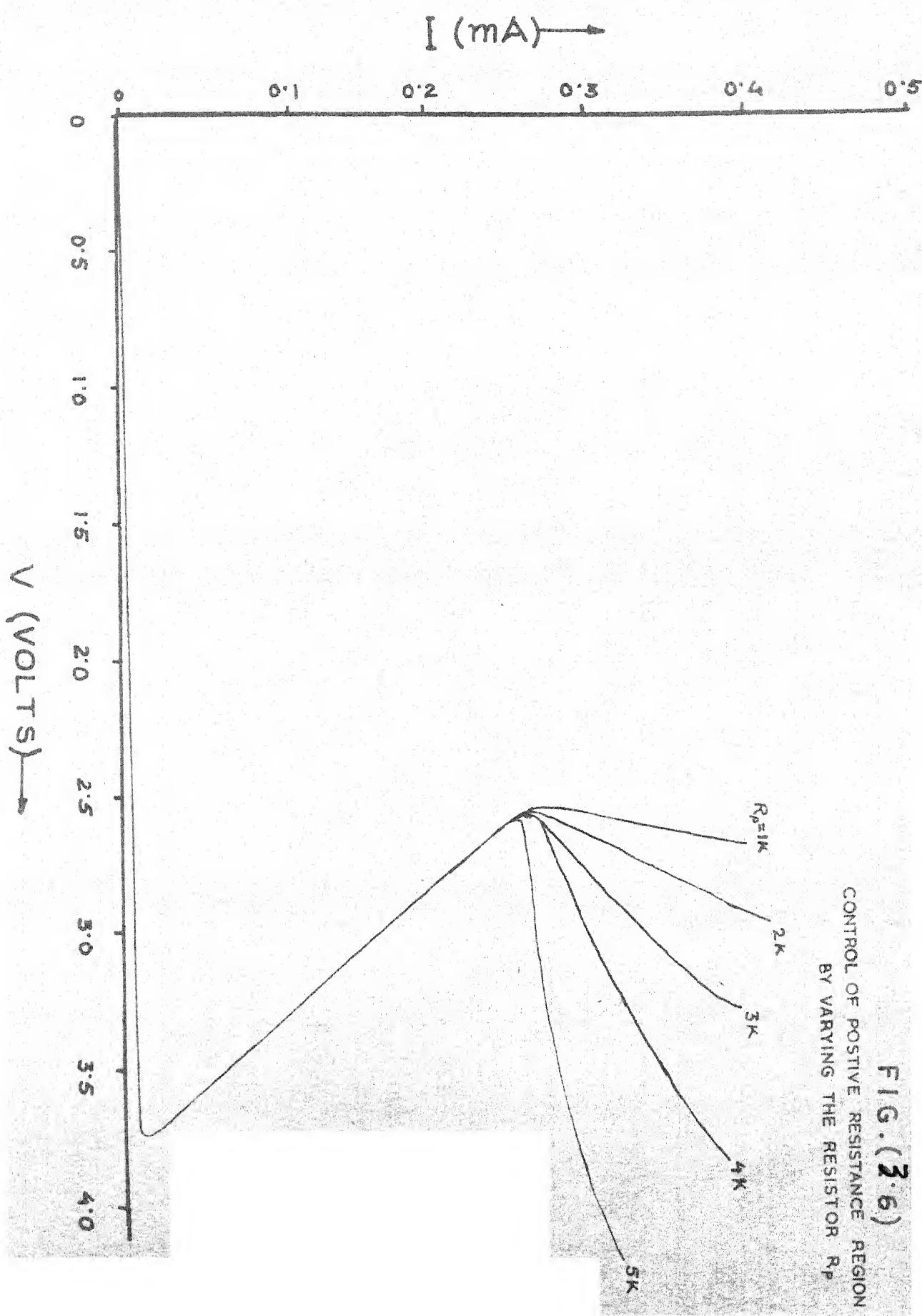
$I(\text{mA})$  —

FIG.(3.5)  
CONTROL OF NEGATIVE RESISTANCE  
BY VARYING THE RESISTOR  $R_N$



voltage variation is small resulting in less non-linearity. One method to reduce the  $\beta$  dependence of current gain and to increase the output impedance, is to use the Wilson's current mirrors [4] shown in Figure (3.7). This will have a current gain given by

$$\frac{I_1}{I_2} = 1 + \frac{2}{\beta^2 + 2\beta} \quad (3.1)$$

A complete circuit employing Wilson's current mirrors is shown in Figure (3.8). The i-v characteristics of this circuit are found to be quite linear as seen from the experimental results shown in Figures 3.9, 3.10, 3.11, 3.12.

### 3.7 Effect of temperature Variation

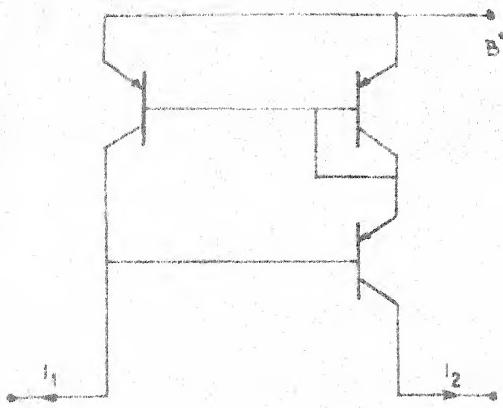
Since the current gain of the mirrors is  $\beta$  dependent and  $\beta$  varies with temperature; even if  $R_N$  and  $R_p$  were held constant, the input resistance looking into node A (Figure 3.13) is slightly temperature sensitive. This is investigated experimentally by raising the temperature of the circuit of Figure (3.8) using an oven. The characteristics (Figure 2.14) show small changes of the order of  $0.1\%/\text{°C}$  in  $R_N$  and  $R_p$ .

With reference to Figure (3.8), the current gains

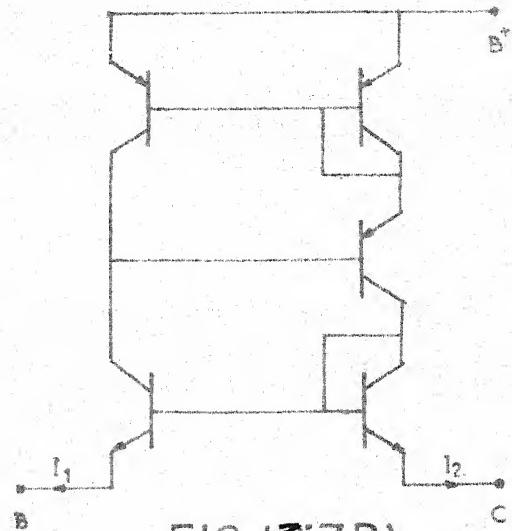
$$\frac{I_1}{I_2} = 1 + \frac{2\beta_1\beta_3 + 2\beta_5\beta_3 - 2\beta_1\beta_5 + 2\beta_1 + 4\beta_3 + 4}{\beta_1\beta_3\beta_5 + 2\beta_1\beta_5 - 2\beta_3 - \beta_3\beta_5 - 2} \quad (3.2)$$

and

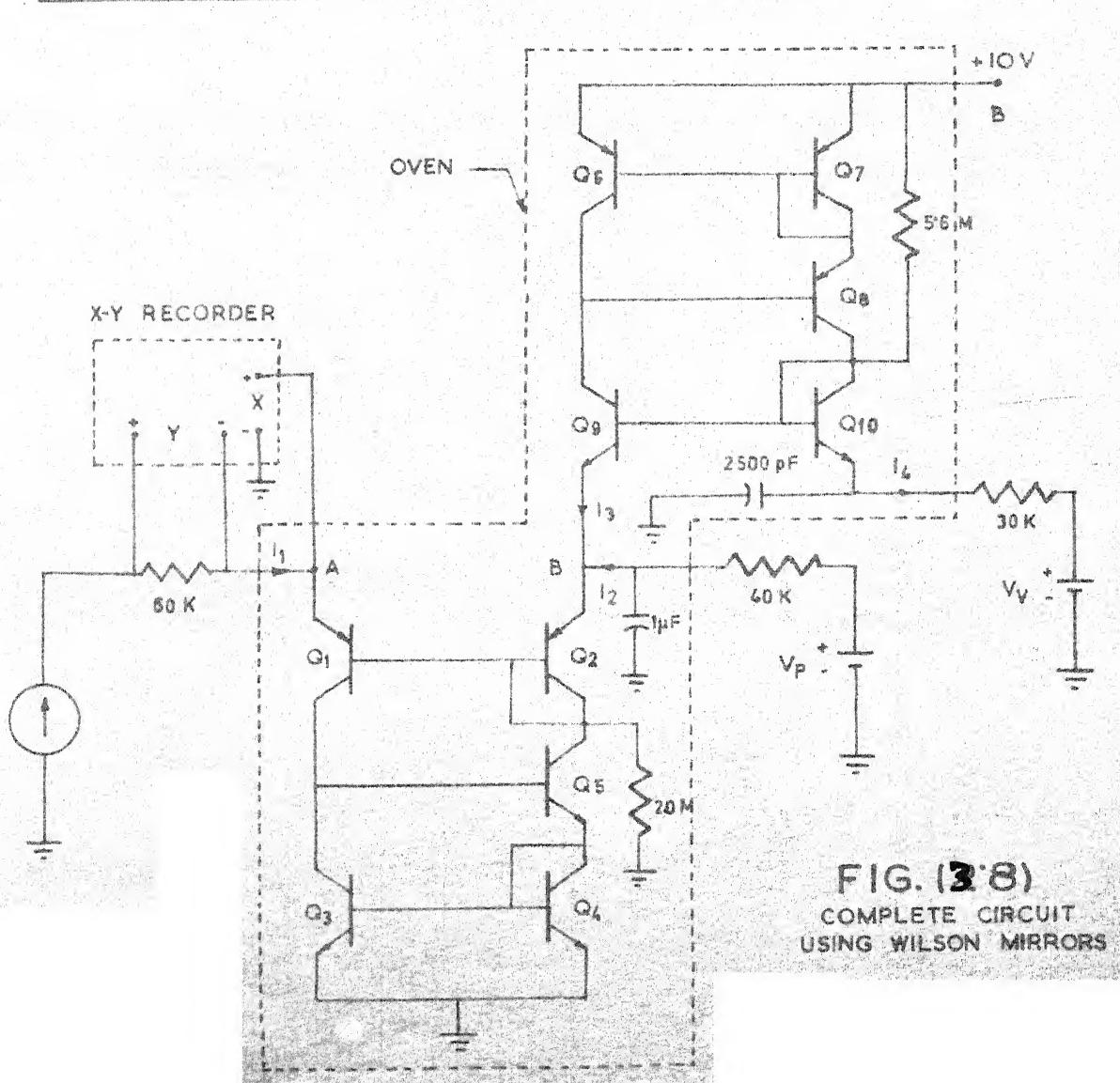
$$\frac{I_3}{I_4} = 1 + \frac{2\beta_9\beta_6 + 2\beta_8\beta_6 - 2\beta_9\beta_8 + 2\beta_9 + 4\beta_6 + 4}{\beta_9\beta_8\beta_6 + 2\beta_9\beta_8 - 2\beta_6 - \beta_8\beta_6 - 2} \quad (3.3)$$



**FIG.(3.7A)**  
WILSON CURRENT MIRROR



**FIG.(3.7B)**  
NIC USING WILSON CURRENT MIRROR



**FIG.(3.8)**  
COMPLETE CIRCUIT  
USING WILSON MIRRORS

FIG. (3.9)

CONTROL OF PEAK VOLTAGE  
IN THE CIRCUIT OF FIG. (28)

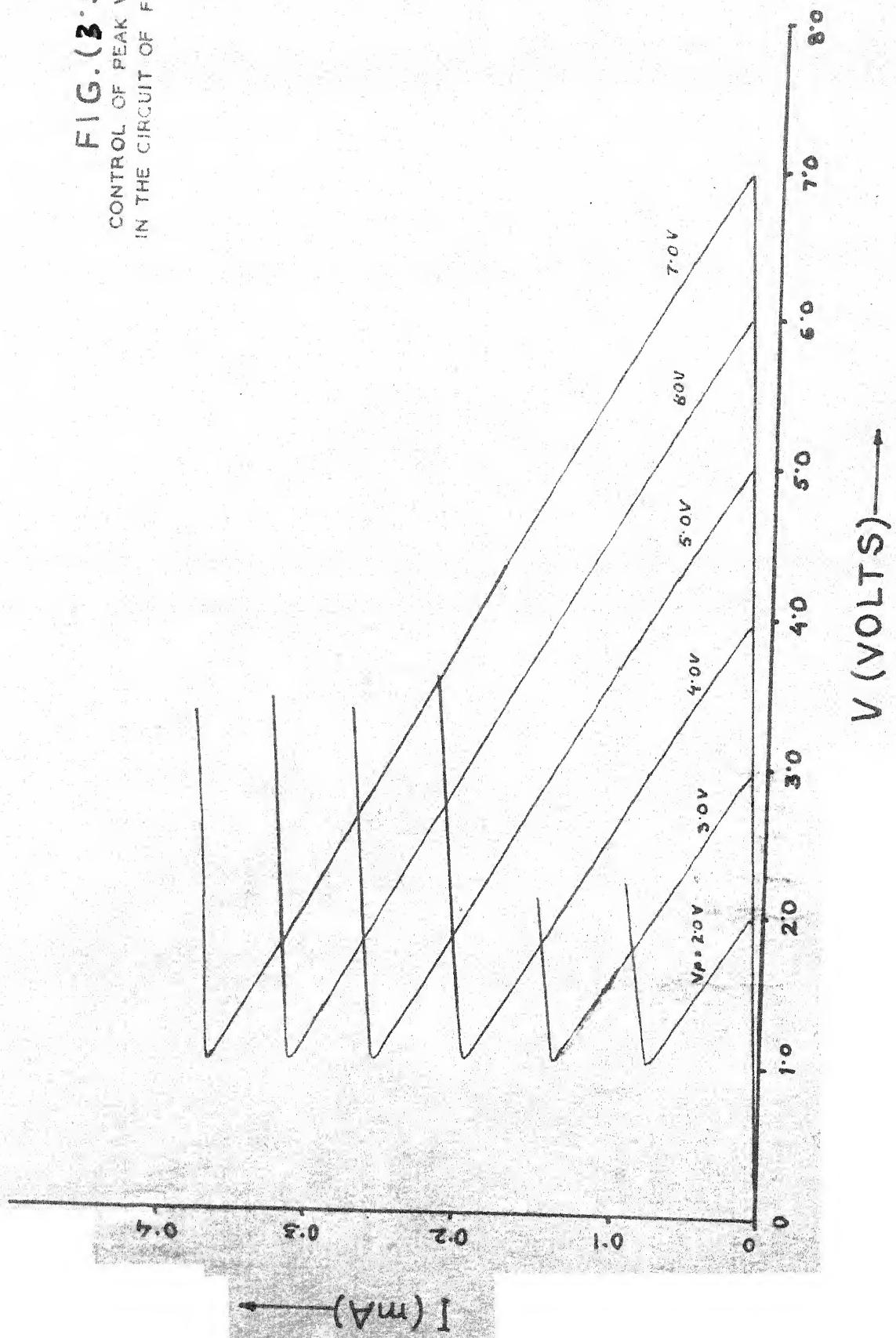


FIG. (3.10)  
CONTROL OF VALLEY VOLTAGE  
IN THE CIRCUIT OF FIG.(2.8)

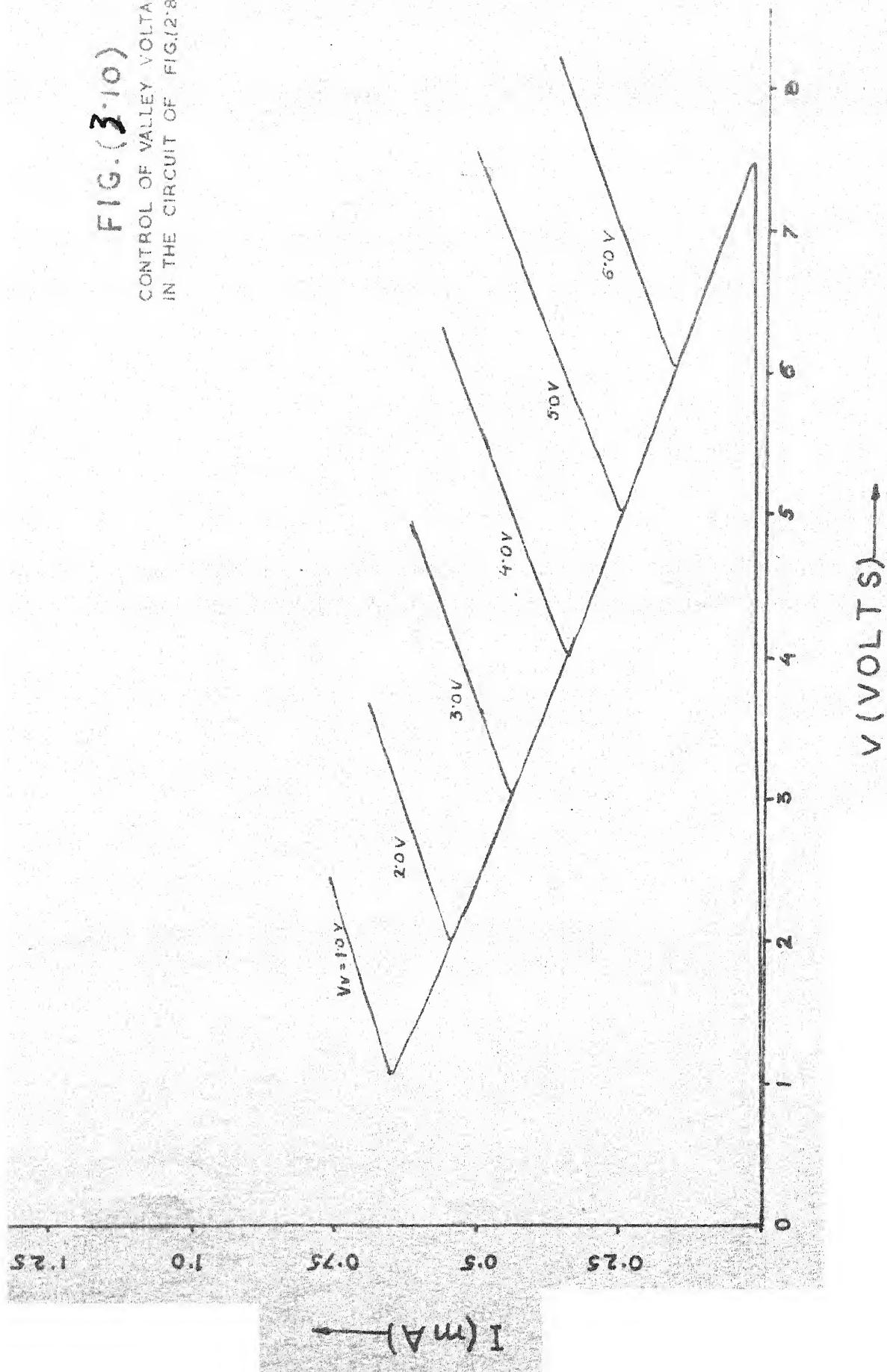
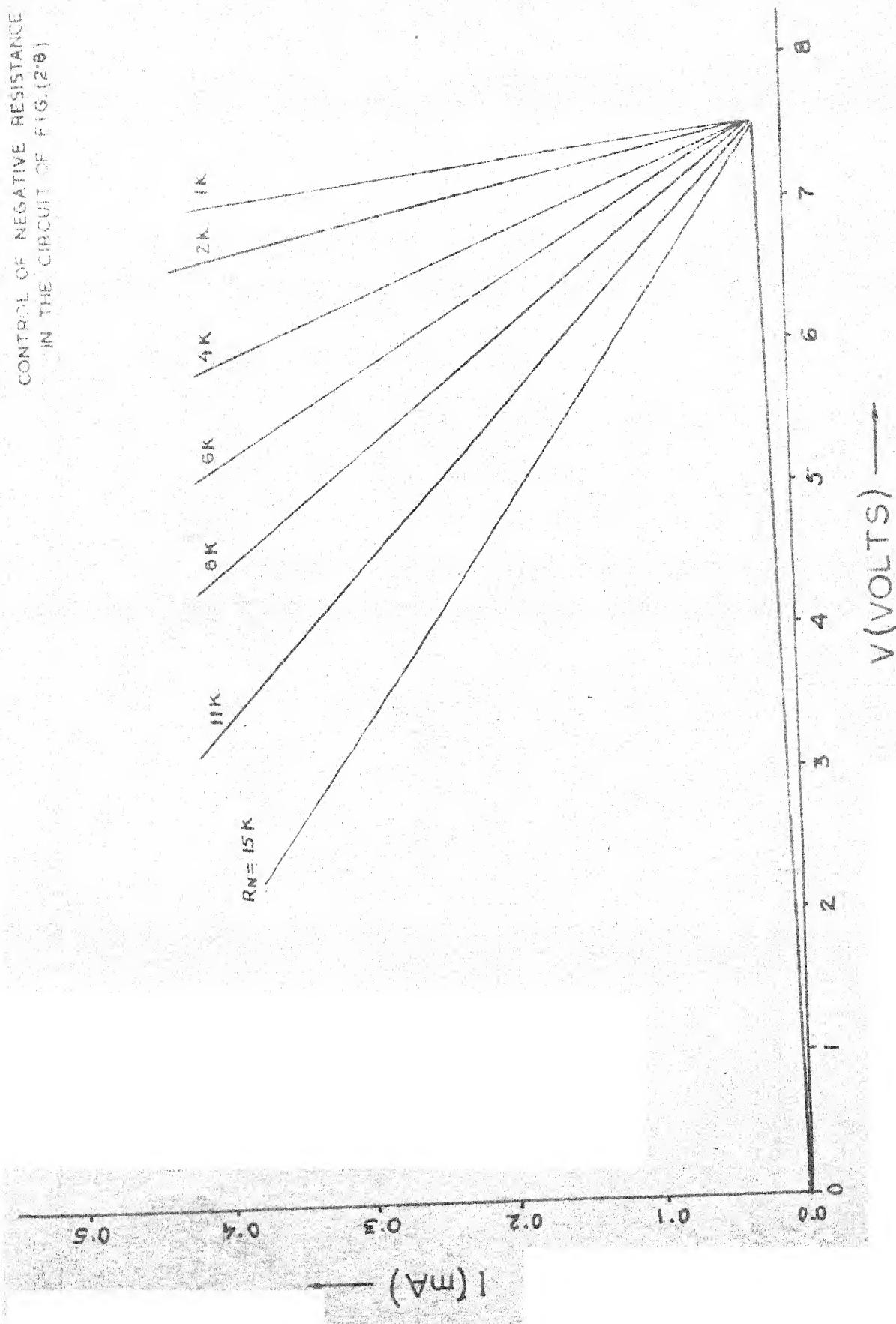
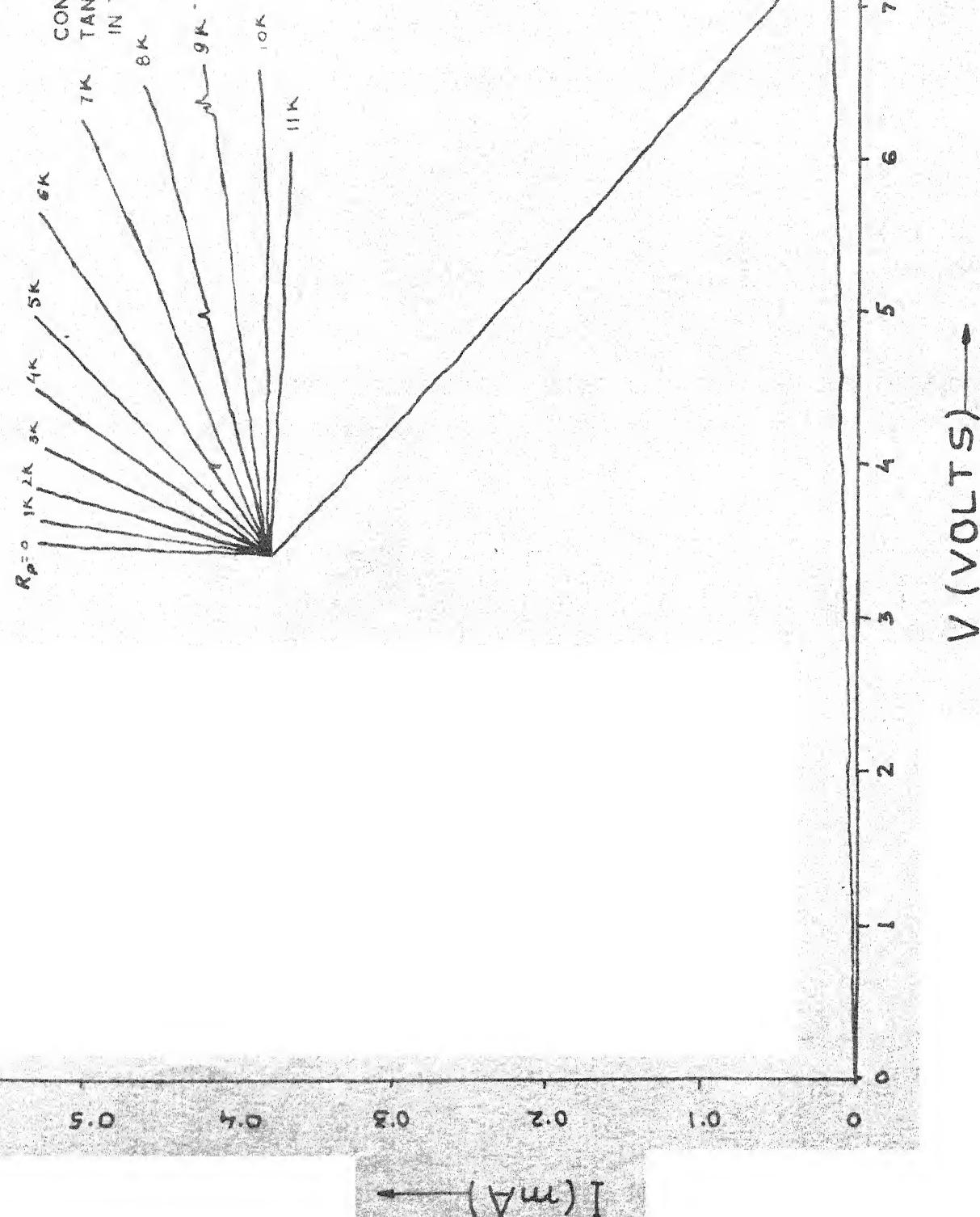


FIG. (31)

CONTROL OF NEGATIVE RESISTANCE  
IN THE CIRCUIT OF FIG.(28)



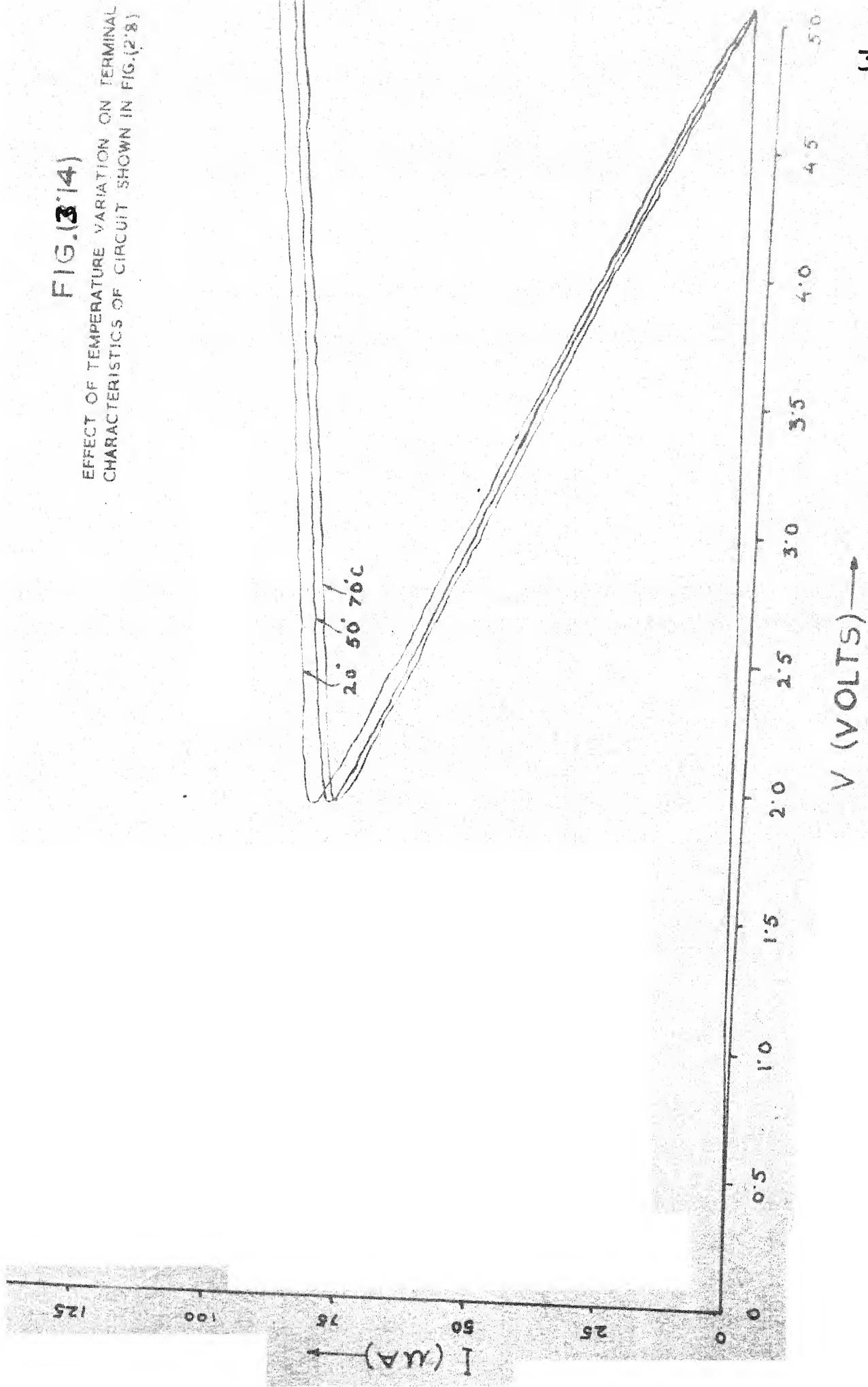
**FIG. (3.12)**  
CONTROL OF POSITIVE RESISTANCE OF THE REGION CD IN THE CIRCUIT OF FIG. (2.8)



33

FIG.(3.14)

EFFECT OF TEMPERATURE VARIATION ON TERMINAL CHARACTERISTICS OF CIRCUIT SHOWN IN FIG.(2.8)



where the subscripts pertain to the respective transistors. If the current gain of all npn transistors is considered to be equal ( $\beta_n$ ) and the gain of all pnp transistors is considered to be equal ( $\beta_p$ ) also if it is assumed that gain of transistors  $Q_1$  and  $Q_9$  tends to infinity the Equation (3.2) and (3.3) will reduce to

$$\frac{I_1}{I_2} = 1 + \frac{2}{\beta_n^2 + 2\beta_n}$$

and

$$\frac{I_3}{I_4} = 1 + \frac{2}{\beta_p^2 + 2\beta_p}$$

Thus under the above conditions, the current gain is less dependent than predicted by Equation (3.2) and (3.3). The temperature sensitivity is expected to be of the order of 90 p.p.m. taking the typical values (from the specification sheets) of  $\beta_n$  and variation of  $\beta_n$  with change in temperature from 25°C to 70°C.

Further improvement is investigated by increasing the current gain by Darlington connection of transistors  $Q_1$ ,  $Q_2$ ,  $Q_9$ ,  $Q_{10}$ . The modified circuit is shown in Figure (2.15). It is seen from the i-v characteristics of circuit 1, of Figure 2.15 (Figure 2.16) that the conversion of  $R_N$  into an equivalent negative resistance is quite temperature insensitive.

To obtain a temperature independent conversion factor of unity the gain of the mirror should be unity. This can be achieved by adding resistors  $R_3$  and  $R_4$  (shown dotted in Figure 2.15) and adjusting them to obtain unity gain.

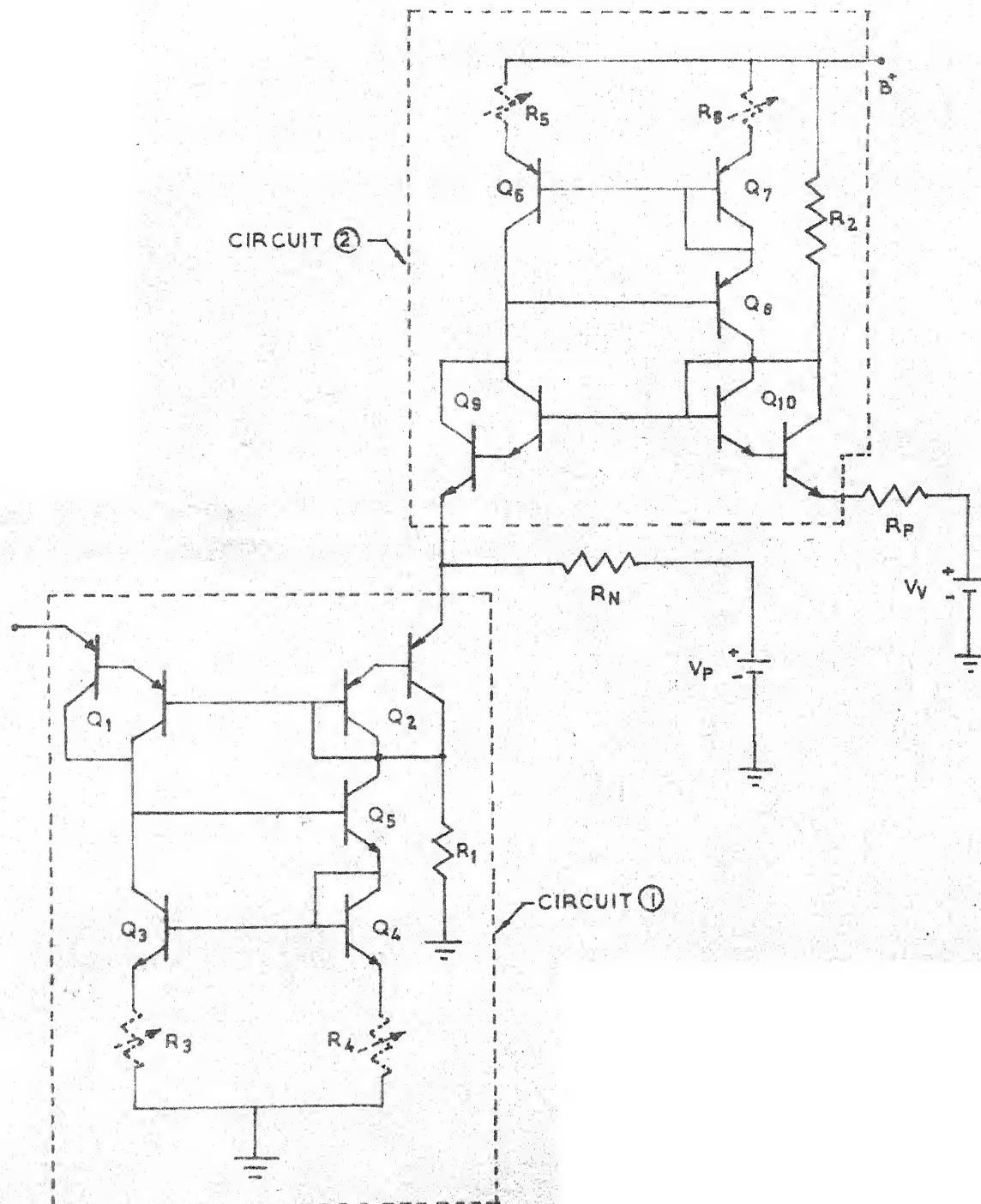


FIG. (3.15)  
CIRCUIT CONTAINING DARLINGTON CONNECTED TRANSISTORS

FIG. (2.16)  
TEMPERATURE DEPENDENCE OF TERMINAL  
CHARACTERISTICS OF CIRCUIT OF FIG.(2.15)

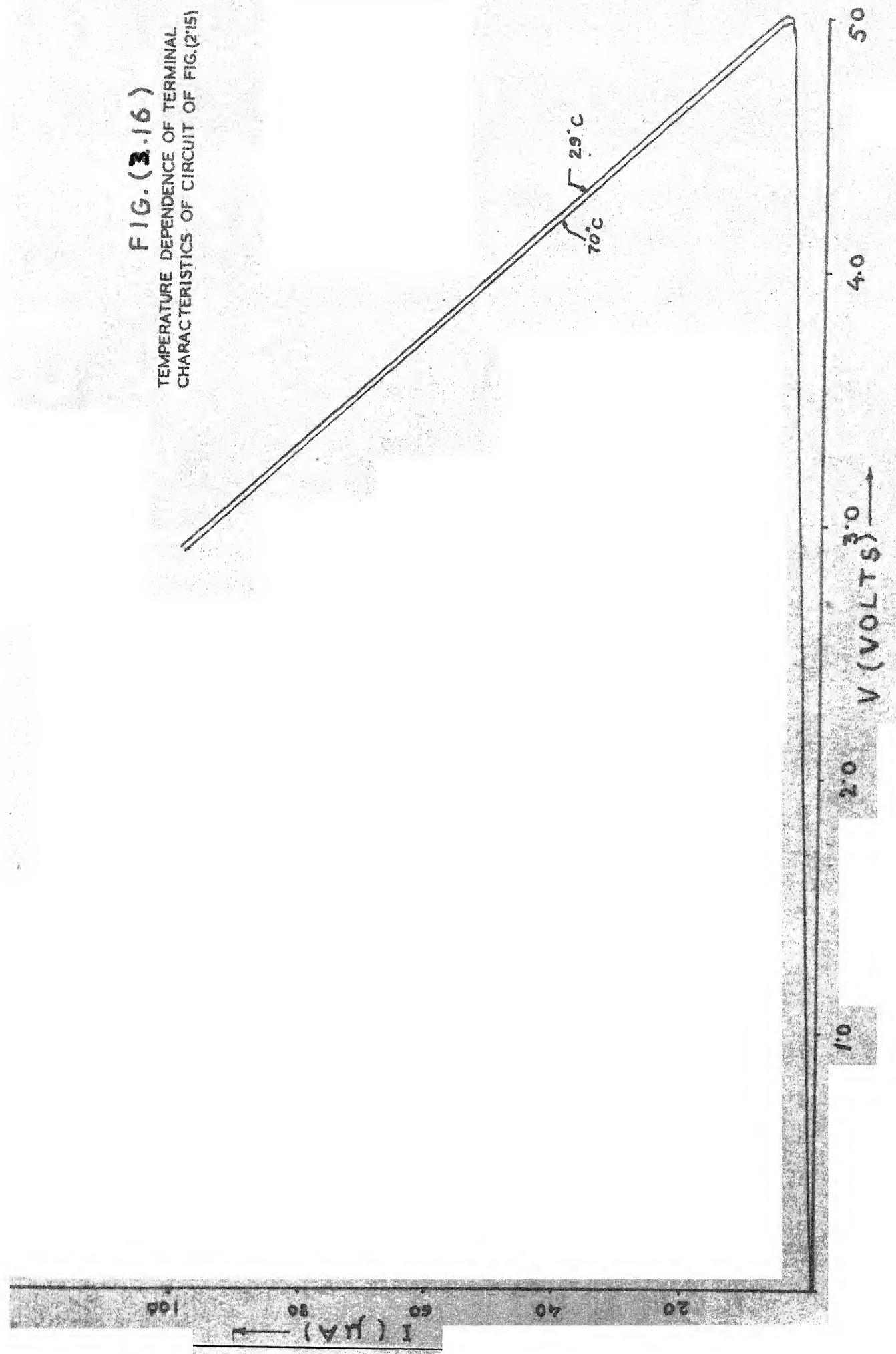
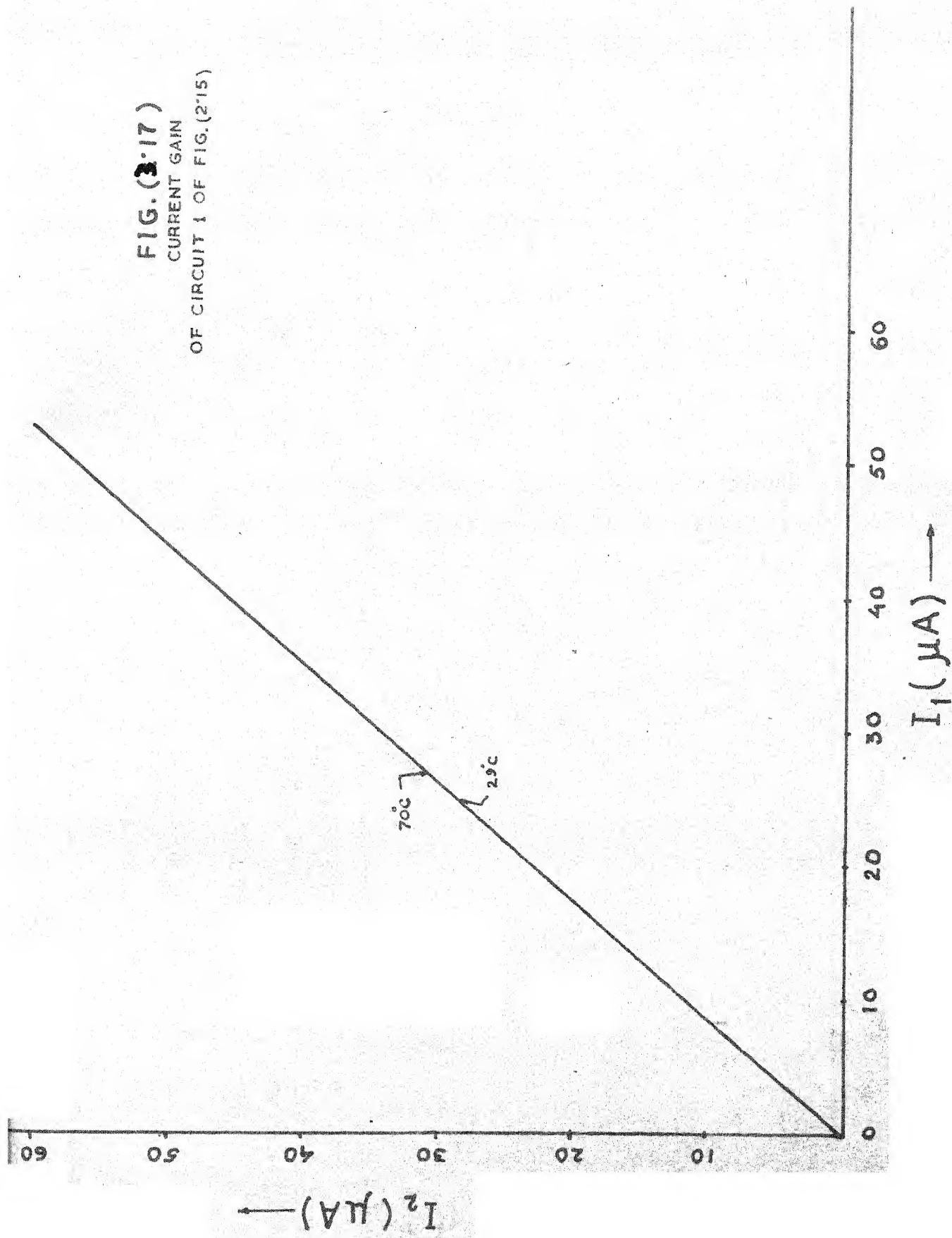


FIG. (3.17)  
CURRENT GAIN  
OF CIRCUIT 1 OF FIG. (2.15)



A similar modification and adjustment is done in  
the circuit 2.

## CHAPTER 4

### OSCILLATOR PERFORMANCE

#### 4.1 Circuit Configuration

In the previous chapters we have seen as to how the i-v characteristics of a practical CCNR circuit can be made to approach that of an ideal pwL characteristics with controlled  $V_p$ ,  $V_v$ ,  $R_N$  etc by making the circuit more and more complex. However, for the experimental study of a relaxation oscillator, a very simple circuit configuration was used to determine the performance (temperature stability of the period of oscillation) that can be achieved.

The circuit diagram is shown in Figure 4.1.  $Q_1$  forms the input transistor.  $Q_2, Q_3, Q_4$  and  $Q_5$  (CA 3086) form a current mirror of nominal gain 3. In order to compensate for the voltage drop of the emitter-base junction of the transistor  $Q_1, Q_6, Q_7$  and  $Q_8$  are used in the configuration shown in the Figure (See Appendix : CA 3084 has this structure available on the chip which is used to advantage). Thus the resistance of 40K appears as -120K (nominal) at the input terminals.  $V_p$  and  $V_v$  are defined using the resistor-divide-chain.

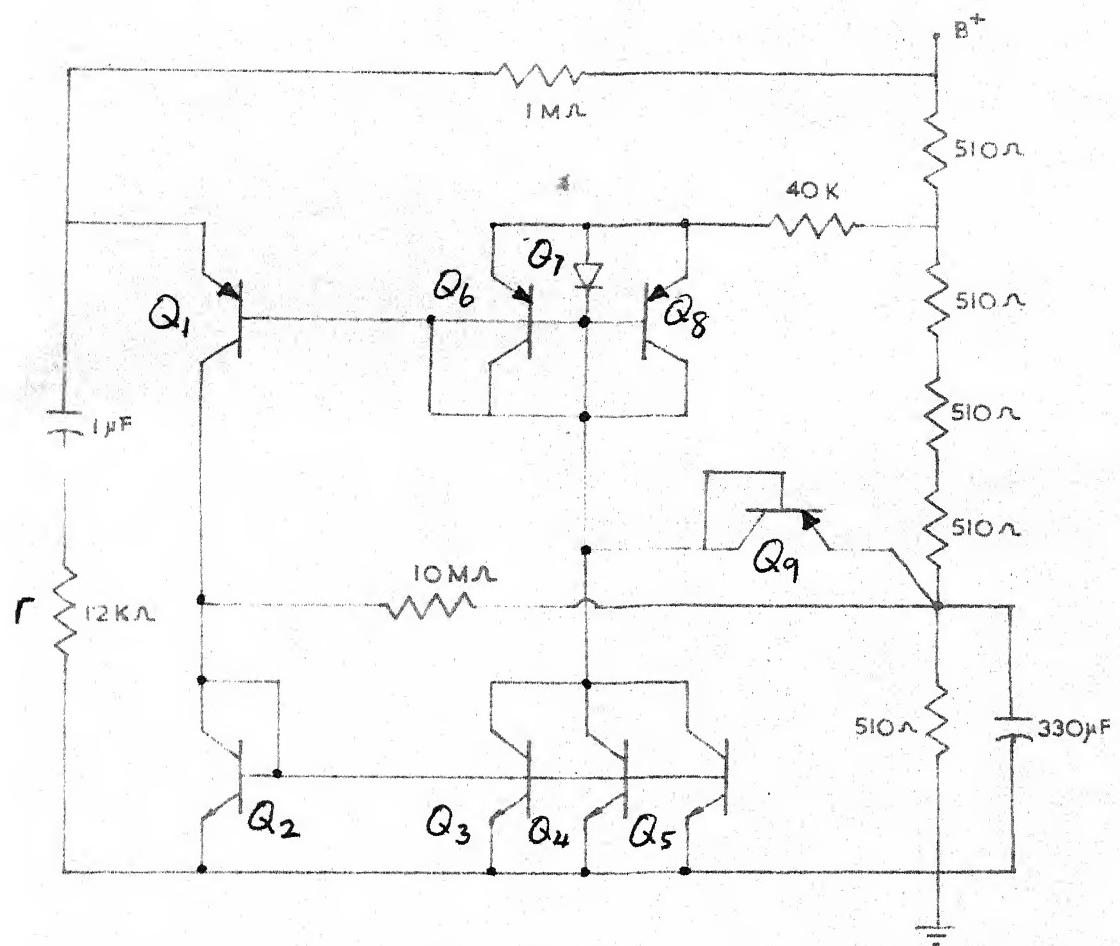


FIG.(4.1d)

RELAXATION OSCILLATOR  
USING SIMPLE CCNR CIRCUIT

The transistor  $Q_9$  is used to clamp the valley voltage approximately. It may be mentioned that this is an alternative by which the complementary NIC can be avoided especially when  $R_p \neq 0$  is desired (positive  $R_p$  can never be achieved this way). The temperature compensation, however, is not exact because the current flowing through  $Q_1$  and  $Q_9$  will never be exactly equal. But the max discharge current of the capacitor (limited by  $V$ ) can be large (depending upon the choice of  $V$ ), and thus the difference between the currents through the  $\text{N}-\text{P}$  junctions of  $Q_1$  and  $Q_9$  are different only by an amount equal to  $I_v$  which is kept in the order of 10 to  $100\mu\text{A}$ .

The  $10\text{M}\Omega$  resistor connected as shown bleeds a small quiescent current through the mirror as well as  $Q_6, Q_7$  and  $Q_8$  which is to prevent the overshoot around the peak voltage (as in the earlier circuits).

The use of a nominal gain of three in the mirror enables us to use a lower resistance to define  $R_N$  which reduces the power supply pick up as well as the voltage drop across the resistors due to reverse saturation currents as well as the current due to the  $10\text{M}\Omega$  resistor. A higher gain could be used with advantage but due to the restriction of the number of devices available on the CA 3084 chips this could not be employed.

#### 4.2 Period of Oscillation

It can be seen from Figure (4.1b) that the region CD is almost vertical due to the clamping provided by the transistor  $Q_9$ . Neglecting the switching time, the period of oscillation is primarily governed by the time taken for the capacitor to

charge from  $V_v$  to  $V_p$  assuming that  $\gamma$  is negligibly small ( $10\Omega$ ). If  $r$  is the order of kilohms, the switching trajectory will be as shown by the dotted lines in Figure 4.1b. Under these conditions, the period of oscillation will be reduced since the voltage ~~max~~ across the capacitor has to change only from  $V_p$ , to  $V_B$ .

If the resistance  $r$  is negligibly small, the period of oscillation for the scaling shown in Figure 4.1(a) will be  $\tau \ln_e \frac{V}{V_p}$ . The period is measured by the arrangement shown in Figure 4.2 where the sharp negative pulse across  $r$  during the discharge of the capacitor, is fed to the counter. It is experimentally observed that power line pick up, even if it is of the order of a millivolt will produce fluctuations in counts because its influence of  $V_p$  is obvious. The high level impedance at the base of the transistor  $Q_1$  before it conducts can be very high. Thus extreme care has to be used in shielding the circuit using a metallic container.

#### 4.3 Influence of $I_{e0}$ of $Q_1$ on the Period of Oscillation

As was pointed out earlier, while the capacitor is charging, the emitter-base junction of the transistor  $Q_1$  is reverse-biased. Its ~~max~~ collector-base junction is reverse biased as well. The base is operated from a high impedance voltage source. Under these conditions, the current flowing into the emitter can be computed using ~~be~~s-Moll relations and it will be in the order of  $I_{e0}$ . Typical value of  $I_{e0}$  measured is in the range of 0.1 na. Considering that the average charging

current is in the order of tens of micro-ampres, the influence of this is expected to be less than 1 part in  $10^5$ . Although a first order compensation of this can be achieved, this was not attempted.

It was experimentally found that the short-term stability of the circuit was controlled by random fluctuations around the peak and valley voltages. Since the voltage difference between the peak and valley voltages is 6V (for a supply voltage of 10V), random drift around the peak and valley voltages of the order  $6\mu V$  will produce fluctuations in the period by an amount equal to 1 part in  $10^6$  which is easily measured. The measured short-term stability (count to count) was in the order of one part in  $10^5$ . The stability of the peak and valley points have to be determined separately by suitable experiments. However, this has not been done. It is envisaged that the randomness around the peak would be dominating factor in the short-term stability. Since the circuit is in a high impedance state around  $V_p$  whereas around  $V_v$ , the devices carry a fair ~~sufficient~~<sup>of</sup> amount current.

#### 4.4 Variation of the Period of Oscillation with Temperature

The variation of the period with temperature was studied by cooling their integrated transistor arrays alone to ice temperature. The results are as given below:

Period measured at room temperature  $25^\circ C$       1352.11 msecs

Period measured at room temperature  $25 \pm 1^\circ C$       1354.91

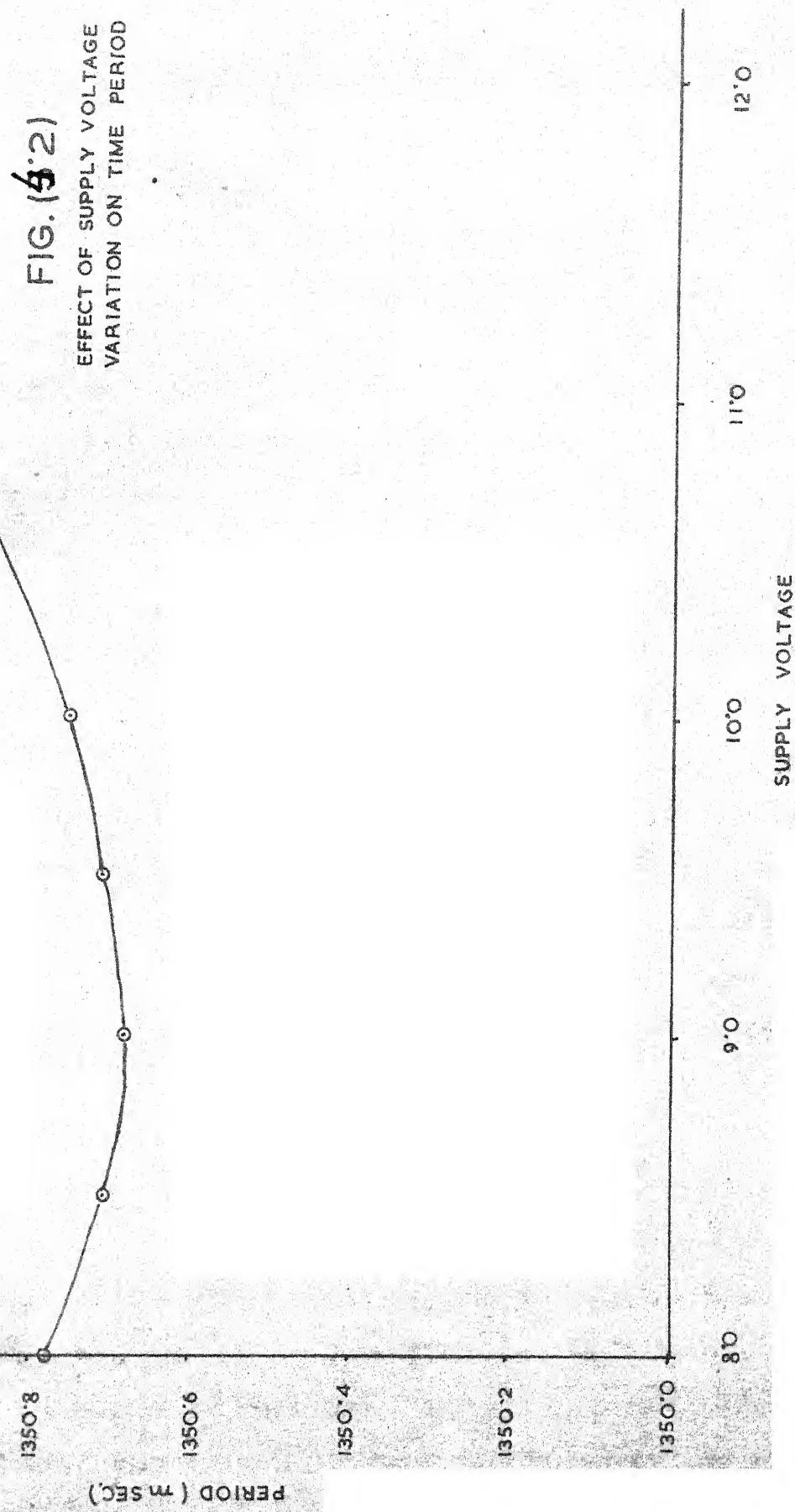
Thus the variation was 2.8 msecs in 1352 msecs which is approximately 86 ppm/ $^\circ C$ . Since the saturation currents increase with temperature, the tendency for the peak voltage will be ~~to~~

to decrease with increase in temperature. Further the reverse saturation current of the emitter-base junction of  $Q_1$  adds to the charging current. Thus, these effects add and make the period of oscillation decrease with temperature. The  $V_{BE}$  effects cancell because of the compensation scheme employed. Thus the experimental observation is consistent with the expected behaviour.

#### 4.4 Variation of the Period of Oscillation with Supply Voltage

The variation of the period as a function of the supply voltage was determined experimentally. Table 4.1 shows the results. The small variation really confirms that the peak and valley voltages vary linearly with the supply voltage. The small variation, however, is due to the non-linear effects such as the voltage dependence of the transistor parameters. This has not been computed using theoretical models. The variation in the period due to supply voltage change is estimated to be 75 ppm/volt (min)

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## CHAPTER 5

### CONCLUSION

The design of oscillators based on piece-wise linear CCNR, results in simple circuit configurations. Except for the timing elements, the circuit can be fabricated in integrated circuit form where the technology is used to advantage in obtaining the temperature compensated performance. While the present investigations show that the circuit is not good enough for watches, the circuit bridges a wide gap between the high precision crystal oscillators and ordinary multivibrators for many industrial timing applications. The quiscences can be made minimal which makes the circuit attractive for battery operated applications. No attempt has been made to match the temperature coefficients of the timing elements R and C which have to be done in order to investigate further improvement of the instability arising from the semi-conducter devices. As is clear, the compensation philosophy based on matching of the transistors in the circuit. There are several more complex circuits which have to be investigated which would need computer-aided analysis. With the advent of ion-implanatation techniques, the degree of matching reported are incredibly low (a few microvolts in  $V_{BE}$  at quiescent current levels as high as 1 ma). The lateral pnp transistors are well behaved at the low current levels they are employed.

The circuit configurations were restricted by the transistor arrays that were available. Thus the present study was restricted to simple structures and by and large the investigations were experimental and analysis very often qualitative.

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APPENDIX A  
GENERAL-PURPOSE HIGH-CURRENT N-P-N TRANSISTOR  
ARRAY

CA3083

Features

High  $I_C$ : 100mA max.

Low  $V_{CEsat}$  (at 50 mA): 0.7V max.

Matched pair (Q1 and Q2) -

$V_{IO} (V_{BE} \text{ matched})$ :  $\pm 5\text{mV}$  max.

$V_{IO}$  (at 1mA): 2.5mA max.

5 independent transistors plus separate substrate  
connection.

Figure A1: Functional diagram of the CA3083

Maximum Ratings, Absolute-Maximum Values at  $T_A = 25^\circ\text{C}$

Power Dissipation:

Any one transistor	500	mW
Total package	750	mW
Above $25^\circ\text{C}$ Derate linearly	6.67	mW/ $^\circ\text{C}$

Ambient Temperature Range:

Operating	-40 to +85	$^\circ\text{C}$
Storage	-55 to +150	$^\circ\text{C}$

## A.2

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage ( $V_{CEO}$ )	15	V
Collector-to-Base Voltage ( $V_{CBO}$ )	20	V
Collector-to-Substrate Voltage ( $V_{CIO}$ )*	20	V
Emitter-to-Base Voltage ( $V_{EBO}$ )	5	V
Collector Current ( $I_C$ )	100	mA
Base Current ( $I_B$ )	20	mA

\*The collector of each transistor of the CA 3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

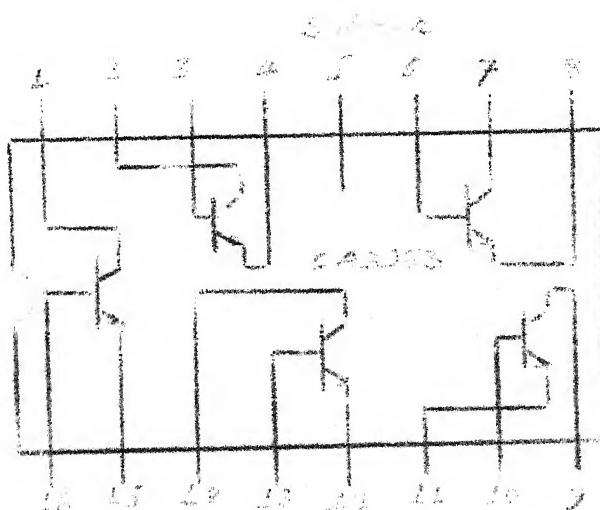


Fig. A2 Functional diagram of the CA3083

ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ C$   
For Equipment Design

Character- istics	Symbol	TEST CONDITIONS		LIMITS			
		Typ. Char. Curve Pig. No.		Min.	Typ.	Max.	Units
<u>For Each Transistor</u>							
Collector- to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C=100\mu A, I_E=0$	-	20	60	-	V
Collector- to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C=1mA, I_B=0$	-	15	24	-	V
Collector- to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI}=100\mu A, I_B=0$	-	20	60	-	V
Emitter-to- Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 500\mu A, I_C=0$	-	5	6.9	-	V
Collector- Cutoff- Current	$I_{CEO}$	$V_{CE}=10V, I_B=0$	-	-	-	10	$\mu A$
Collector- Cutoff- current	$I_{CBO}$	$V_{CB}=10V, I_E=0$	-	-	-	1	$\mu A$
DC Forward- Current Transfer Ratio	$h_{FE}$	$V_{CE}=3V$	$I_C=10mA$ $I_C=50mA$	2	40	76	-
Base-to- Emitter Voltage	$V_{BE}$	$V_{CE}=3V, I_C=10mA$	3	0.65	0.74	0.85	V
Collector- to-Emitter Saturation Voltage	$V_{CESat}$	$I_C=50mA, I_B=5mA$	4	-	0.40	0.70	V

Character- istics	Symbol	TEST CONDITIONS			LIMITS		
		Typ.	Char.	Min.	Typ.	Max.	Units
		Curve					
		Fig.					
		No.					
<b>For Transistors Q1 and Q2 (As a Differential Amplifier):</b>							
Absolute Input Offset Voltage	$V_{IO}$		7	-	1.2	5	mV
Absolute Input Offset Current	$I_{IO}$	$V_{CE} = 3V, I_C = 1mA$	8	-	0.7	2.5	$\mu A$

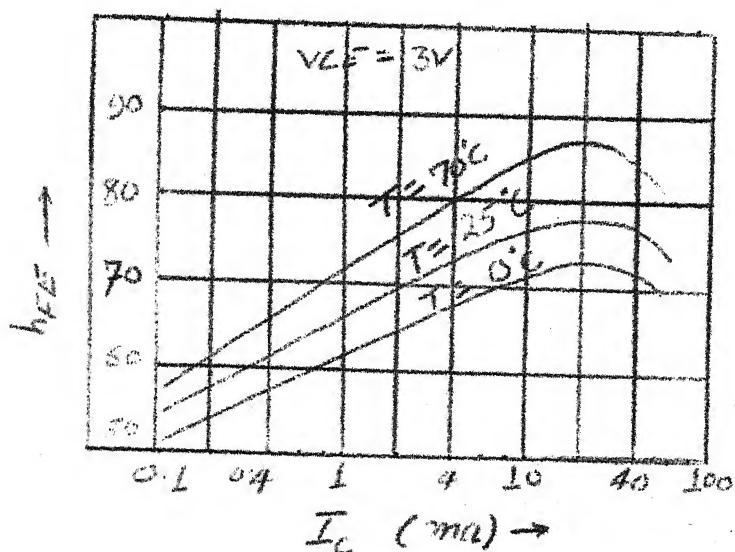


Fig A2:  $h_{FE}$  v.  $I_C$

APPENDIX B  
GENERAL-PURPOSE P-N-P TRANSISTOR ARRAY  
**CA3084**

Features

Matched transistor pair (Q1 and Q2)

$V_{IO}(V_{BE} \text{ matched})$ :  $\pm 6\text{mV}$  max.

$I_{IO}$  (at 100 A) :  $\pm 0.6\mu\text{A}$

Wide operating current range

Low noise figure 3.2dB typ. at 1kHz

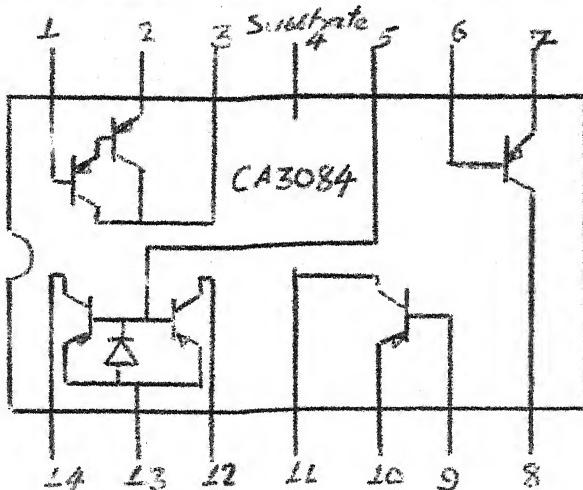


Figure B1: Functional Diagram of the CA3084.

ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$

		TEST CONDITIONS					
CHARACTERS	SYMBOL	Typ.	Charac-	LIMITS	Unit:		
			teris-	Min.	Typ.	Max.	
			ties				
			Curve				
			Fig.No.				

For Each Transistor:

Collector- Cutt-off current	$I_{CBO}$	$V_{CB} = -10\text{V}, I_E = 0$	2	- -0.055	-100	mA
-----------------------------------	-----------	---------------------------------	---	----------	------	----

CHARACTERS	SYMBOL	TEST CONDITIONS			LIMITS		
		TYP.	Charac.	Min.	Typ.	Max.	Units
Collector-Cutoff Current	$I_{CBO}$	$V_{CE} = -10V, I_E = 0$	2	-	<del>±125</del> -0.12	-100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_{CE} = 100\mu A, I_B = 0$	-	-40	-70	-	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_{CB} = 100\mu A, I_E = 0$	-	-40	-80	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_{EB} = 100\mu A, I_C = 0$	-	-40	-100	-	V
Emitter-to-Substrate Breakdown Voltage	$V_{(BR)EIO}$	$I_{EI} = 100\mu A$	-	-40	-100	-	V
Collector-to-Emitter Saturation Voltage	$V_{CESat}$	$I_E = 1mA, I_B = 100\mu A$	4	-	-0.125	-0.25	V
Base-to-Emitter Voltage	$V_{BE}$		5	<del>15</del> -0.50	<del>50</del> -0.59	-	V
DC Forward h <sub>FE</sub> Current Transfer Ratio	$h_{FE}$	$I_E = 100\mu A, V_{CE} = -10V$	7	15	40	-	
For Transistor Q1 and Q2 (As a Differential Amplifier)							
Magnitude of Input Offset Voltage	$ v_{IO} $		8	-	0.422	6	mV
Input Offset Current	$I_{IO}$	$I_E = 100\mu A, V_{CE} = -10V$	-	-0.6	0	0.6	μA

CHARACTERISTICS		TEST CONDITIONS		LIMITS		U
	SYMBOL	Typ.	Charac-	Min.	Typ.	Max.n
		teris-	ties			i
		Curve				s
		Fig.No.				

For Transistors Q3 and Q4 (Current-Mirror Configuration)

Collector Current	$I_C$	$V_{CE} = -10V, V_{CIO} = -10V$	10	0.85	1.00	1.15	$\mu A$
Magnitude of Collector Current Ratio	$ I_C(Q3)/I_C(Q4) $	Term. 13 = Gnd. $I_5 = -100\mu A$	11	0.90	1.00	1.10	

For Transistors Q5 and Q6 (Darlington Configuration)

Collector-Cutoff Current	$I_{CEO}$	$V_{CE} = -10V, I_B = 0$	-	-	-	-	$\mu A$
Base-to-Emitter Voltage	$I_{CEO}$		13	0.92	1.07	1.20	V
DC Forward Current Transfer Ratio	$h_{FE}$	$I_E = 100\mu A, V_{CE} = -10V$	15	100	1230	-	

ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ C$   
Typical Values Intended Only for Design Guidance

Magnitude of Temperature Coefficient

$V_{BE}$ (for each transistor)	$ \Delta V_{BE}/\Delta T $	$I_E = 100 \mu A, 6$	-1.78	$mV/^\circ C$
$V_{IO}$ (as a differential amplifier)		$V_{CE} = -10V 9$	0.54	$\mu V/^\circ C$
$V_{BE}$ (Darlington configuration)	$ \Delta V_{BE}/\Delta T $	14	-3.7	$mV/^\circ C$

For Each Transistor:

Input Resistance	$R_I$	$f = 1kHz, V_{CE} = -10V$	19	-	9	$k\Omega$
Output Resistance	$R_O$		20	-	600	$- k\Omega$
Forward Transconductors	$S_m$	$I_C = 100\mu A$	22	-	3	$- mho$

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		Typ.	LIMITS	U n t s
		Charac- teris- ties Curve Fig.No.	Min. Typ. Max.i			
Collector- to- Base- Capacitance	$C_{CBO}$	$I_{CB} = 0$	23	-	3.3	- pF
Collector- to-Emitter Capacitance	$C_{CEO}$	$I_{CE} = 0$	23	-	2.5	- pF
Base-to- Substrate Capacitance	$C_{BIO}$	$I_{CIO} = 0$	23	-	4.5	- pF

MAXIMUM RATINGS, Absolute-Maximum Values at  $T_A=25^\circ C$ 

## Dissipation:

Any one transistor	200	mW
Total package	750	mW
Above $T_A=55^\circ C$ derate linearly	6.67	mW/ $^\circ C$

## Ambient Temperature Range:

Operating	-40 to +85	$^\circ C$
Storage	-55 to +150	$^\circ C$

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage ( $V_{CEO}$ )	-40	V
Collector-to-Base Voltage ( $V_{CBO}$ )	-40	V
Base-to-Substrate Voltage ( $V_{BIO}$ )*	-40	V
Emitter-to-Base Voltage ( $V_{EBO}$ )	-40	V
Collector Current ( $I_C$ )	-10	mA

\*The base of each transistor of the CA3084 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any base voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (4) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

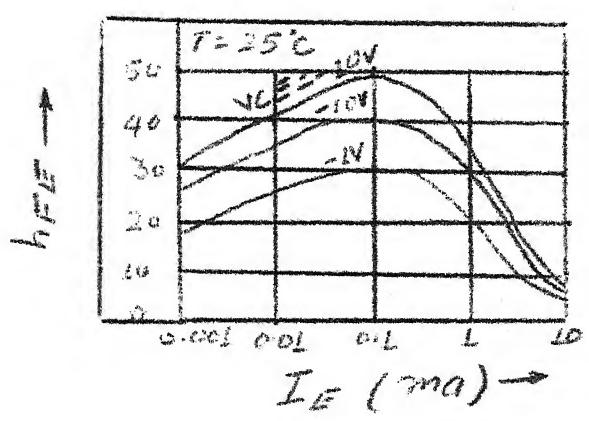
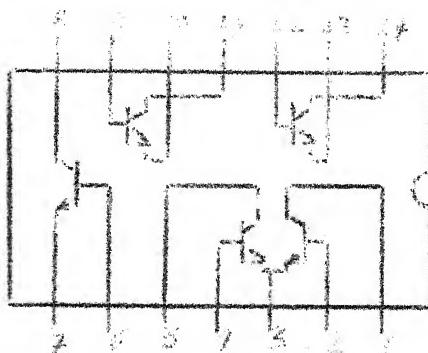


Fig. B2:  $h_{FE}$  Vs.  $I_E$

APPENDIX C  
GENERAL-PURPOSE N-P-N TRANSISTOR ARRAY  
CA3086

**Three isolated Transistors and One Differentially Connected Transistor Pair**

**For Low-Power Applications from DC to 120MHz**



**Figure C1: Functional Diagram of the CA3086.**

**MAXIMUM RATINGS, Absolute Values (Maximum) at  $T_A = 25^\circ\text{C}$**

**Dissipation:**

Any one transistor	300	mW
Total package	750	mW
Above $T_A=25^\circ\text{C}$ derate linearly	6.67	mW/ $^\circ\text{C}$

**Ambient Temperature Range:**

Operating	-40 to +85	$^\circ\text{C}$
Storage	-55 to + 150	$^\circ\text{C}$

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, $V_{CEO}$	15	V
Collector-to-Base Voltage, $V_{CBO}$	20	V
Collector-to-Substrate Voltage, $V_{CIO}^*$	20	V
Emitter-to-Base Voltage, $V_{EBO}$	5	V
Collector Current, $I_C$	50	mA

\*The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ C$ 

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			Typ. Charac- teris- tics Curves Fig.No.	LIMITS	U n i t s
		Min.	Typ.	Max.			
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C=10\mu A; I_E=0$	-	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C=1mA, I_B=0$	-	15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C=10mA, I_CI=0$	-	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E=10\mu A, I_C=0$	-	5	7	-	V
Collector-cutoff Current	$I_{VBO}$	$V_{CB}=10V, I_E=0$	2	-	0.002 100 nA		
Collector-Cutoff Current	$I_{CEO}$	$V_{CE}=10V, I_B=0$	3	-	Curve 5 nA	See Curve	
DC Forward Current Transfer Ratio	$h_{FE}$	$V_{CE}=3V, I_C=1mA$	4	40	100	-	

ELECTRICAL CHARACTERISTICS at  $T_A=25^\circ C$   
Typical Values Intended Only to Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS			U n i t s
		Typ.	Charac- teris- ties	Typical Values	
DC Forward- Current Transfer Ratio	$b_{FE}$	$V_{CE}=3V$	$I_C=10mA$	4	100
			$I_C=10\mu A$	4	54
Base-to- Emitter Voltage	$V_{BE}$	$V_{CE}=3V$	$I_E=1mA$	5	0.715 V
			$I_E=10mA$	5	0.800 V
$V_{BE}$ Temperature coefficient	$\Delta V_{BE}/\Delta T$	$V_{CE}=3V$ , $I_C=1mA$		6	-1.9 mV/ $^\circ C$
Collector-to- Emitter Satura- tion Voltage	$V_{CESat}$	$I_B=1mA$ , $I_C=10mA$		-	0.23 V
Noise Figure (low frequency)	$N_F$	$f=1kHz$ , $V_{CE}=3V$ , $I_C=100\mu A$ , $R_S=1k\Omega$		-	3.25 dB
Low-Frequency, Small-Signal Equivalent- Circuit Characteris- tics					
Forward Current Transfer Ratio	$h_{fe}$			7	100 -
Short-Circuit Input Impedance	$h_{ie}$	$f=1kHz$ , $V_{CE}=3V$ , $I_C=1mA$		7	$3.5 k\Omega$
Open-Circuit Output Impedance	$h_{oe}$			7	$15.6 \mu mho$
Open-circuit Reverse-Voltage Transfer Ratio	$h_{re}$			7	$1.8 \times 10^{-4}$ -
Admittance Characteristics:					
Forward Transfer Ratio	$y_{fe}$			8	$31-31.5 mmho$

TEST CONDITIONS		Typ. Charac- teristi- cs Curves Fig. No.	Typical Values	U n i t s
CHARACTERISTICS	SYMBOL			
Input Admittance $y_{ie}$	$f=1\text{MHz}, V_{CE}=3\text{V}, I_C=1\text{mA}$	9	$0.3+j0.04 \text{ mmho}$	
Output Admittance $y_{oe}$		10	$0.001+j0.03 \text{ mmho}$	
Reverse Transfer Admittance $y_{re}$		11	See Curve -	
Gain-Bandwidth Product	$f_T \quad V_{CE}=3\text{V}, I_C=3\text{mA}$	12	550	MHz
Emitter-to-Base Capacitance	$C_{EBO} \quad V_{EB}=3\text{V}, I_E=0$	-	0.6	pF
Collector-to-Base Capacitance	$C_{CBO}=3\text{V}, I_C=0$	-	0.58	pF
Collector-to-Substrate Capacitance	$C_{CEO}=3\text{V}, I_C=0$	-	2.8	pF

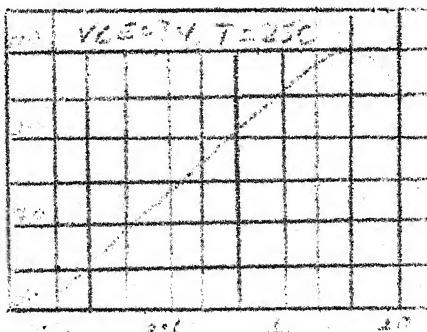


Fig.C2: h<sub>FE</sub> V. I<sub>E</sub>